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Combined Effects of Ionizing Radiation and Electromagnetic Interference: The need of combined tests to achieve reliable systems

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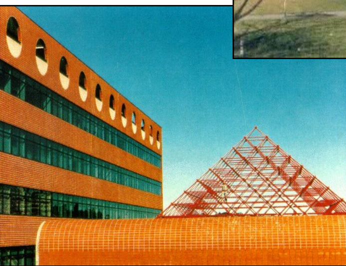

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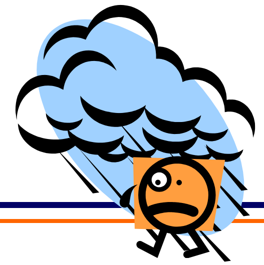
Motivation, Main Concerns



Aerospace Industry

Designers face a continuous pressure to use **new technologies** to improve **performance**, **cost** and **procurement time** for electronic systems devoted to **critical applications** (aerospace).

E.g., replace radiation-hardened ICs by COTS components!

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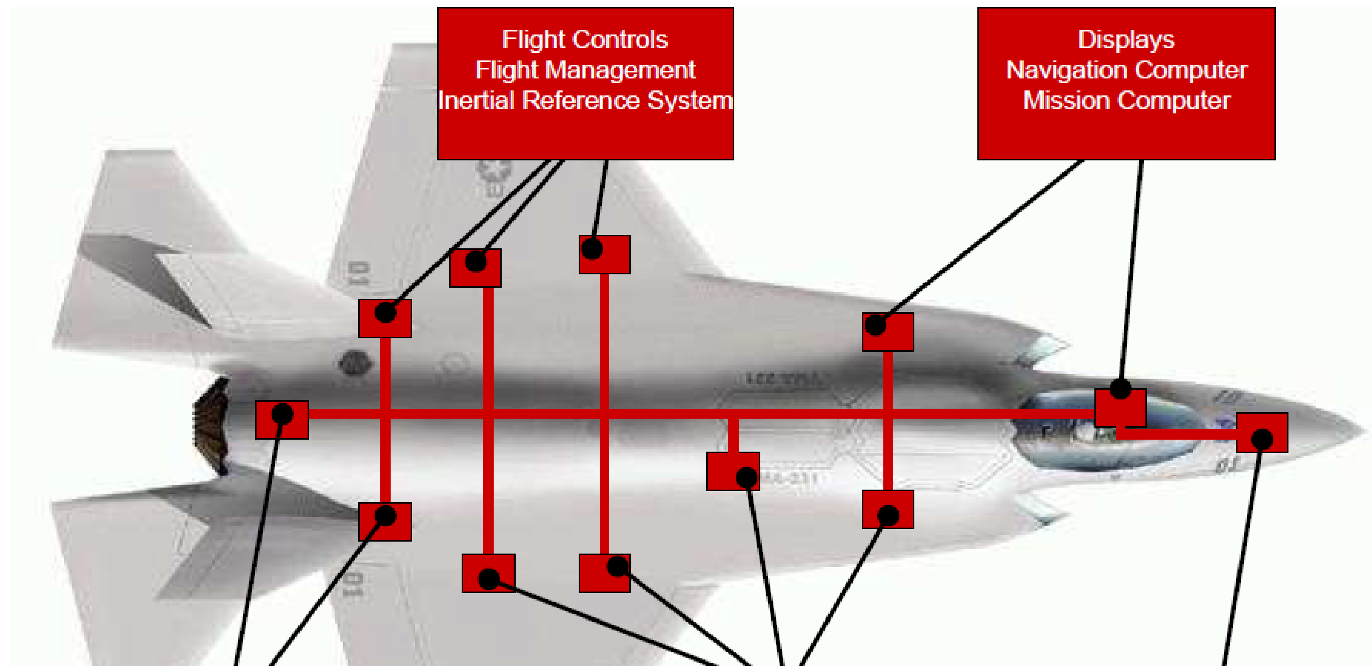
Motivation, Main Concerns

Aerospace Industry

In avionics, most of the designs are moving from the **Federated Architecture: FA** (F-Control, F-Warning, Nav-System, Cabin Pressure, etc…)



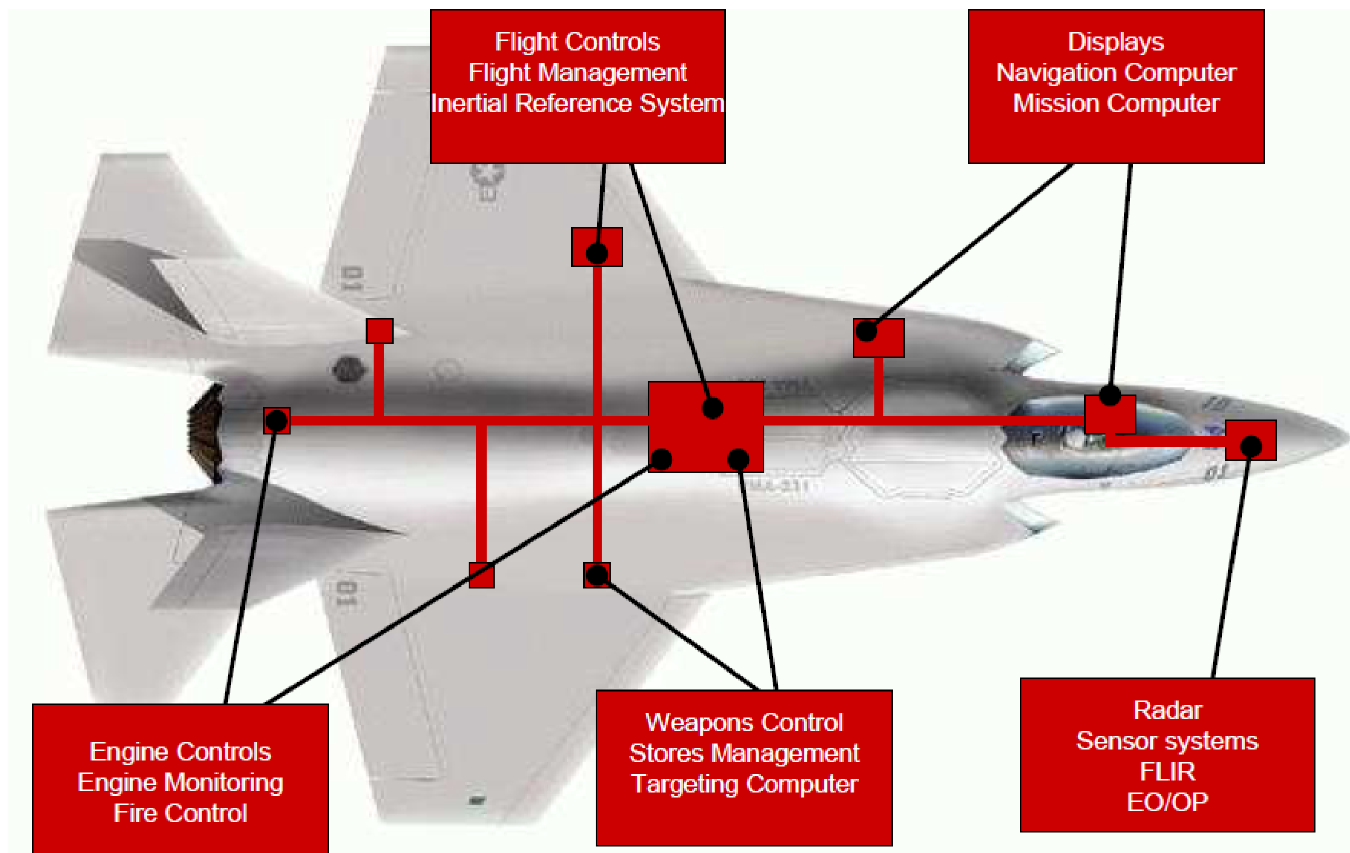
FA approach: no longer feasible by the **continuous growing performance requirements** of modern aircrafts.

Reasons: huge **# of sub-systems** requires **unsustainable maintenance effort** as well as a tremendous budget requirements in terms of size, weight and power consumption (**SWaP**).

Motivation, Main Concerns

Aerospace Industry

to the **Centralized Architecture** (**IMA**: **I**ntegrated **M**odular **A**vionics)
-> *multiple functions with mixed criticality running on a single chip!*



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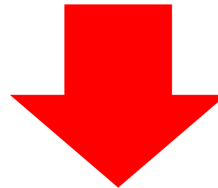
Motivation, Main Concerns

Aerospace Industry

These new architectures require the use of

fast and **reliable ICs** (such as **NoC MPSoC-based systems**,

FPGAs and **memories**) in **mission-critical applications**



which makes **EMI & ionizing radiation control** even

more challenging

Current State-of-the-Art

From the best of our knowledge ...

Only a few works addressing the problem: trying to understand and quantify the combined effects of ionizing (**total-ionizing dose: TID**) and non-ionizing (**EMI**) radiations on ICs

The Effects on Cardiac Pacemakers of Ionizing Radiation and Electromagnetic Interference from Radiotherapy Machines

(Int. Journal of Radiarion Oncology Biol. Phys. Vol. 4. pp. IO55-IO58, 1978)

Pacemaker Failure Due to Radiation Therapy

(PACE. Vol. 5, pp156-159, March-April 1982)

When cancer patients with implanted pacers undergo radiation therapy it is important to known whether the treatment will have any deleterious effects on the pacer, thus placing the patient in jeopardy from malfunction. Malfunction may consist of continuous or intermittent spurious signals or an interruption of normal pacer signals.

Radiation therapy exposes a pacemaker to ionizing radiation alone (60Co), or ionizing radiation plus strong electromagnetic fields (linear accelerators and betatrons), which may induce noise and interference into reactive electronic circuits.

"In our study, the observed ***effect on pacemaker function was severe enough to justify some concern****"*

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Current State-of-the-Art

From the best of our knowledge ...

Electromagnetic Interference and Ionizing Radiation Effects on CMOS Devices
(IEEE TRANS. ON PLASMA SCIENCE, VOL. 40, NO. 6, JUNE 2012)

N- and PMOS devices presented **shift and distortion of the voltage and current transfer characteristics**, leading to **reduced noise margins** and **logic instability**.

"EMI + TID combination *proved most damaging, when compared to* ***isolated*** *EMI and ionizing radiation experiments**"***

None work, except from our group, focused on the combined effects of ionizing (**soft errors in memory elements**) and non-ionizing (**EMI**) radiations on ICs

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Current State-of-the-Art

From the best of our knowledge ...

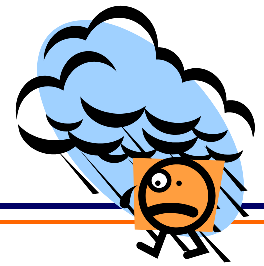
Absence of a **standard** to rule combined tests

(currently, only a Draft Recommendation from ITU:
"Overview of particle radiation effects on telecommunications systems", Geneva, Oct. 2016)

Our studies have shown a **considerable reliability degradation** for systems operating in harsh environments (such as space, where satellite electronics is exposed to the combined effects of ioninzing rad: TID/soft errors and EMI)

(Analysis of SRAM-Based FPGA SEU Sensitivity to Combined EMI and TID-Imprinted Effects, IEEE TRANS. ON NUCLEAR SCIENCE, VOL. 63, JUNE 2016)

Where is the problem?



It is a common practice that …

engineers qualify electronic systems to EMI, TID or SEU, or eventually to all of them, but often NOT taking into account the combined effects one phenomenon may take over the other.

e.g., assume a given part of an embedded system for satellite application is certified by a set of EMI tests according to specific stds

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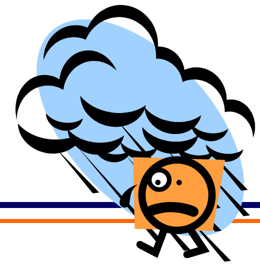
Where is the problem?



After a given period of time [illegible]

Who can ensure that this pa[illegible] will still perform [illegible]rly according to the same set of EMI stds, after a given level [illegible] radiation has been cumulated over time on the system, if the [illegible] certified independently for EMI and radiation?

Moreover, who can ensure that the system will be approved for the same set of EMI stds, if operating in a harsh environment with dense flux of high-energy particles (SEEs)?

How to test/qualify such electronics?

In the light of this problem ...

We ...

- analyze the impact of combined tests for EMI + radiation (TID/SEU) on the reliability of electronic components
- propose a new methodology that takes this combination into account in order to qualify state-of-the-art COTS ICs

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Outline

1. Understand the effects of ionizing radiation (TID, SEU, SEE) & non-ionizing radiation (EMI) on embedded electronics
2. Mitigation techniques
3. Combined test planning
4. Configurable platform and lab requirements for combined test
5. Experiments combining TID + SEU + EMI tests on FPGAs

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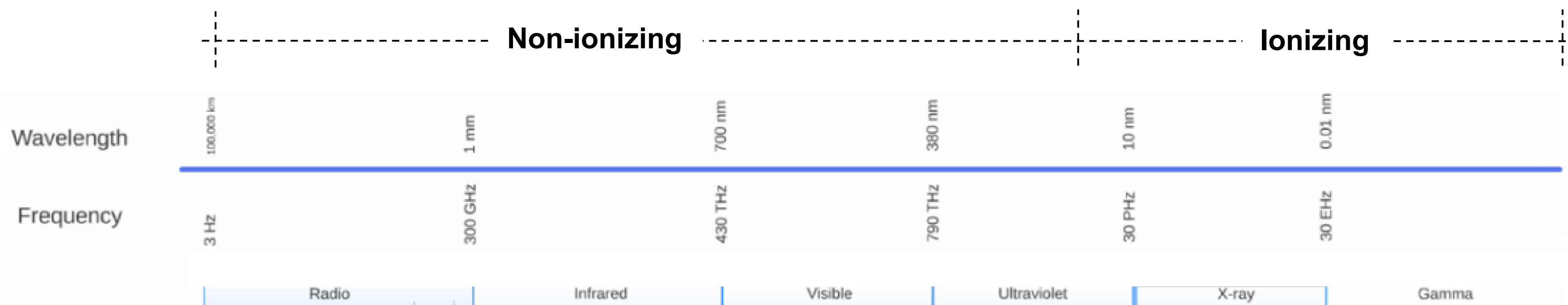
Types of radiation: *Ionizing* X *Non-Ionizing* …

Non-ionizing radiation refers to any type of electromagnetic radiation that does not carry enough energy to **remove** an **electron** from an atom or molecule. Thus, it has energy **only to excite** an electron to a **higher energy state**

On the other hand, **ionizing radiation** **changes** the matter characteristics when passing through it by producing **charged ions**



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1. Understanding the effects of ionizing radiation (TID, SEU, SEE) & non-ionizing radiation (EMI) on embedded electronics

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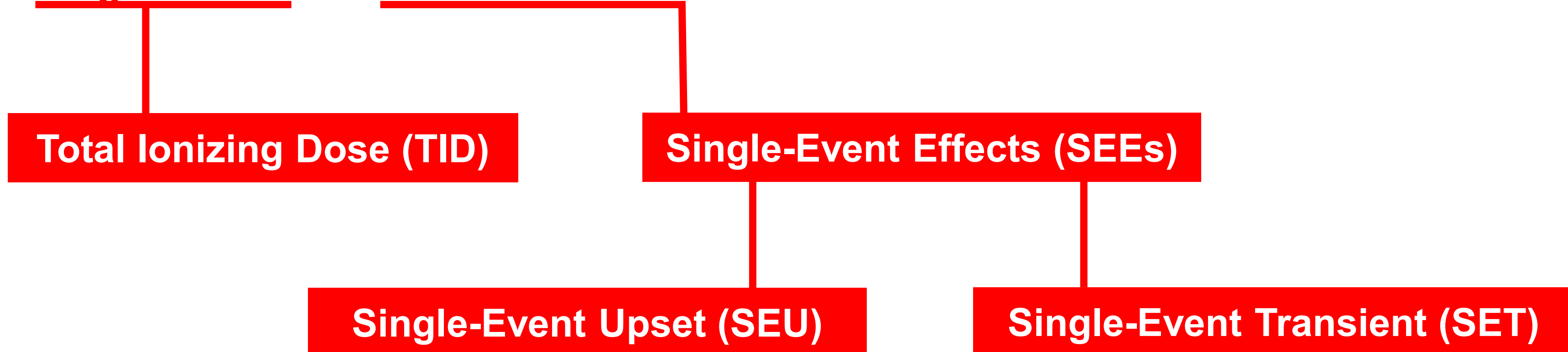
Understanding the Effects of Radiation on Electronics

Mechanisms of radiation interaction can cause a wide variety of changes in circuit & systems' performance

The observed degree of chance depends on the device type and radiation type

It is useful to treat the mechanisms of radiation interaction in terms of long duration and transient effects



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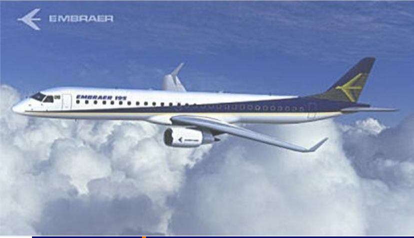
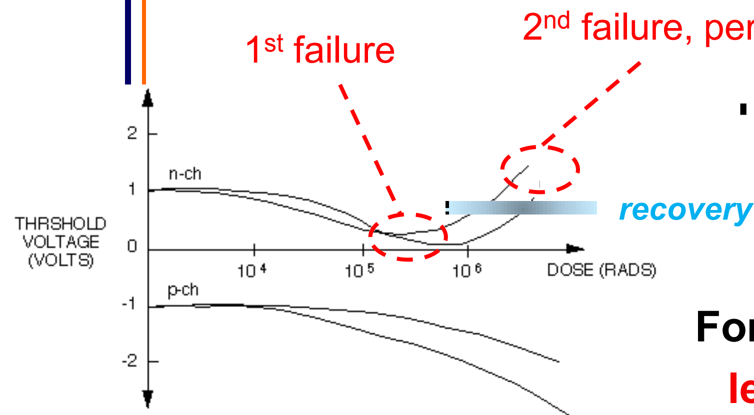


Understanding the Effects of Radiation (TID) on Electronics

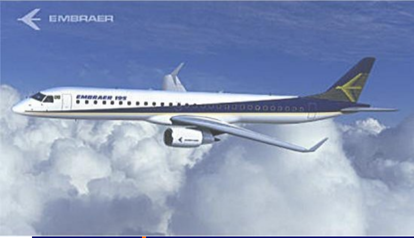
For **critical applications** (military, aerospace or biomedical) reliability assurance to **total ionizing dose (TID) radiation** is always at a premium being a key-issue for the success of such products in the market.



TID effects on CMOS ICs are caused primarily by **positive charge trapped in insulating layers**

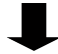
For CMOS ICs, the main TID effect is the **increase of leakage currents** and **change in V_{th}** of the devices

For high doses, a **permanent functional failure** of the circuit is observed.



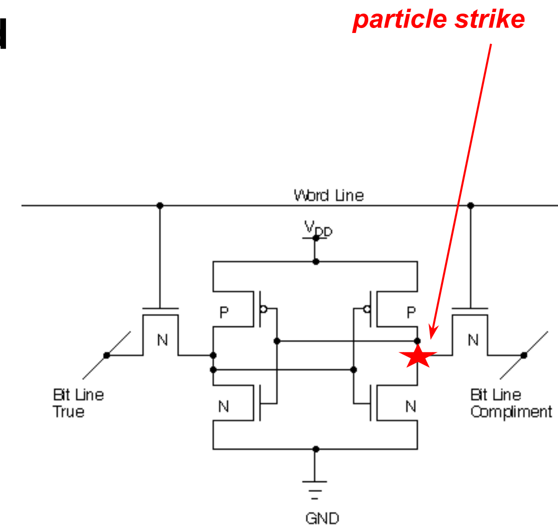
Understanding the Effects of Radiation (SEE) on Electronics

Radiation (SEU) effects on CMOS ICs are mainly caused by **high-energy particles striking reverse biased drain depletion region of off-transistors**



For CMOS ICs, the main SEU effect is the **loss of information stored in memory elements** (FFs, RAMs)

Transient functional failure
of the circuit is observed



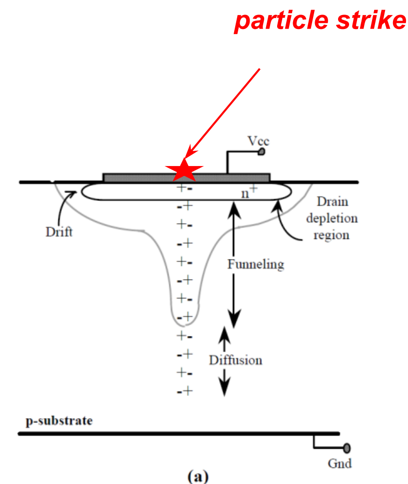
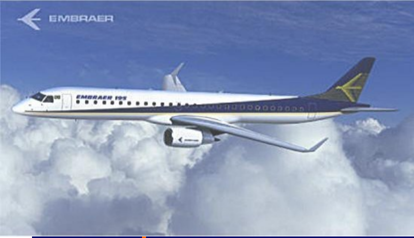


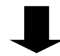
Fig. 1. Illustration of the charge collection mechanism that cause single-event upset: **(a)** particle strike and charge generation; **(b)** current pulse shape generated in the n+p junction during the collection of the charge.



Understanding the Effects of Radiation (SEE) on Electronics

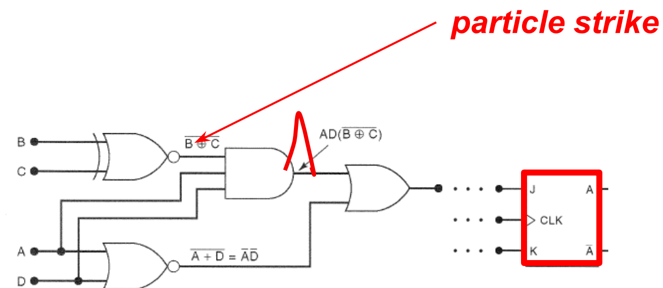
Radiation (SET) effects on CMOS ICs are mainly caused by **high-energy particles striking logic along with critical paths**

For CMOS ICs, the main SET effect is the **loss of information stored in memory elements** (FFs, RAMs)



Transient functional failure
of the circuit is observed

particle strike



Radiation Testing Standards

USA Department of Defense

Test Procedure of MIL-STD-883H - Test Method for Microcircuits

METHOD NO.	ENVIRONMENTAL TESTS
1001	Barometric pressure, reduced (altitude operation)
1002	Immersion
1003	Insulation resistance
1004.7	Moisture resistance
1005.8	Steady state life
1006	Intermittent life
1007	Agree life
1008.2	Stabilization bake
1009.8	Salt atmosphere (corrosion)
1010.7	Temperature cycling
1011.9	Thermal shock
1012.1	Thermal characteristics
1013	Dew point
1014.10	Seal
1015.9	Burn-in test
1016	Life/reliability characterization tests
1017.2	Neutron irradiation
1018.2	Internal water-vapor content
1019.4	Ionizing radiation (total dose) test procedure
1020.1	Dose rate induced latchup test procedure
1021.2	Dose rate upset testing of digital microcircuits
1022	Mosfet threshold voltage
1023.2	Dose rate response of linear microcircuits
1030.1	Preseal burn-in
1031	Thin film corrosion test
1032.1	Package induced soft error test procedure (due to alpha particles)
1033	Endurance life test
1034	Die penetrant test (for plastic devices)

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Radiation Testing Standards

European Space Agency

Agence Spaciale Européenne

TOTAL DOSE STEADY-STATE IRRADIATION

TEST METHOD

ESA/SCC BASIC SPECIFICATION No. 22900

SINGLE EVENT EFFECTS TEST METHOD

AND GUIDELINES

ESA/SCC Basic Specification No. 25100

SCC

space components
coordination group

SISC
PUCRS

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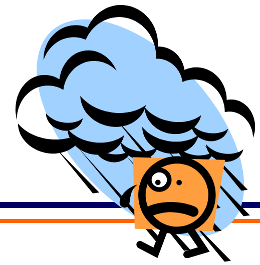
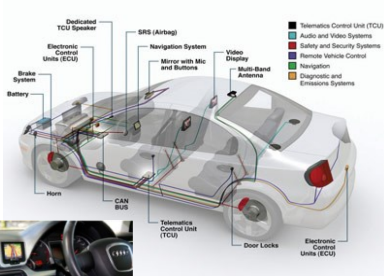
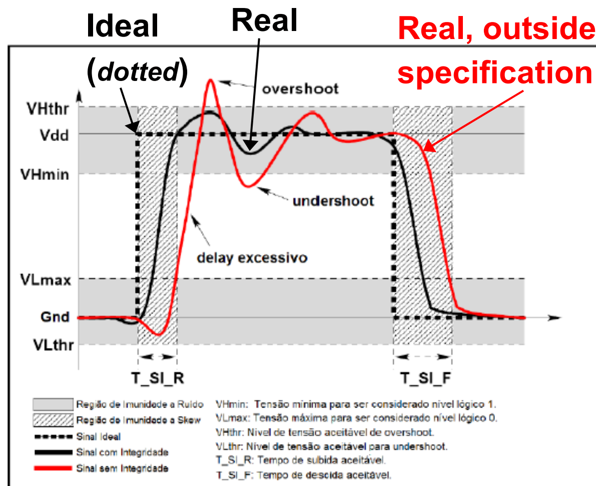
Understanding the Effects of EMI on Electronics



The **increasing hostility of the electromagnetic environment** caused by the widespread adoption of electronics, (mainly **wireless technologies**), represents a huge challenge for the reliability of RT embedded systems.





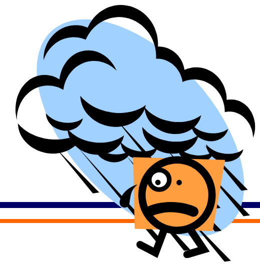
Electromagnetic Interference (EMI)

Power Supply Disturbances (PSD)

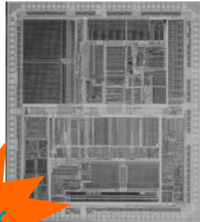
Transient Faults

Signals outside noise margins can be erroneously interpreted and stored by memory elements at the end of critical paths

Understanding the Effects of EMI on Electronics

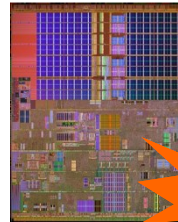


M68000 (1978),
20MHz, 5um, 3.3-5V



~100K

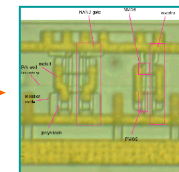
iPentium4 (2006),
4GHz, 65nm, 1.5V



~100M

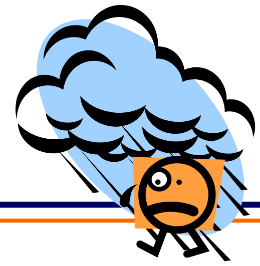
Proc? (2014/2015),
?GHz, 22nm, 0.5-1V

~400M

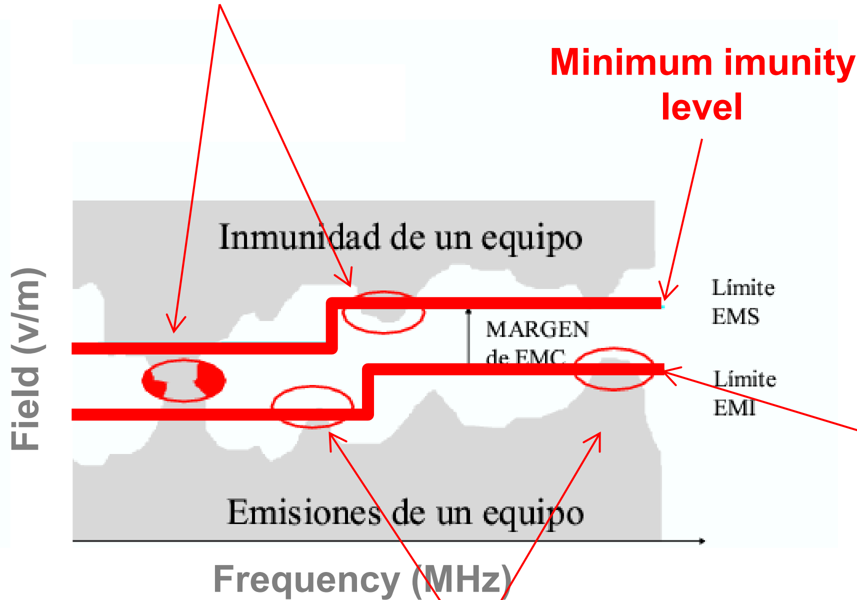


Technology tr…s impact on ICs

Understanding the Effects of EMI on Electronics



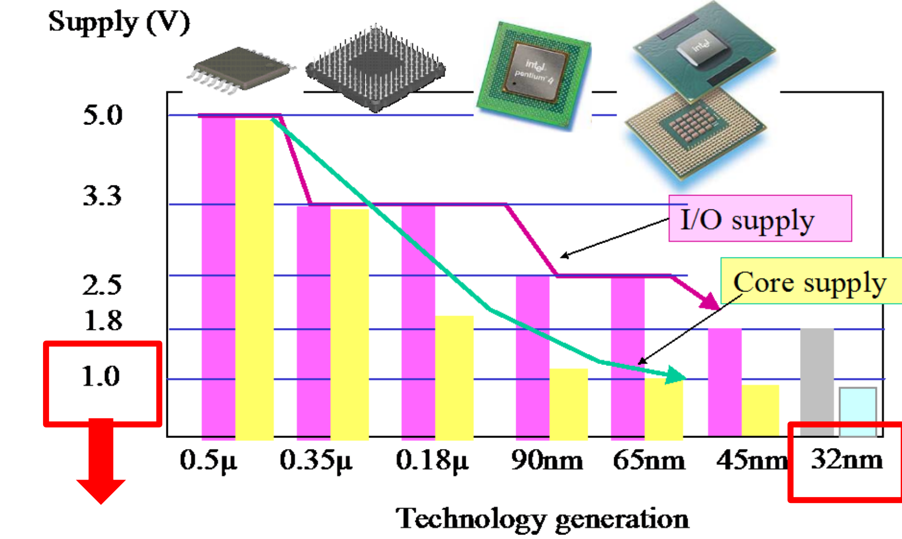
Violation of the Minimum imunity



Minimum imunity level

Maximun emission level

Violation of the Maximun emission



Continuous **reduction of voltage supply** reduces noise margins and thus, **increases susceptibility**

IEC International Standards

System-Level Test

IEC 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4-17: Testing and measurement techniques – **Ripple on d.c. input power port immunity test**.

IEC 61.000-4-29: Electromagnetic compatibility (EMC) – Part 4-29: Testing and measurement techniques – **Voltage dips, short interruptions and voltage variations on d.c. input power port immunity tests**".

IEC 62.132: **Measurements of Electromagnetic Immunity, 150 kHz – 1 GHz**:

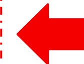
Part 1: General conditions and definitions

Part 2: (G-) TEM Cell Method

Radiated Method

Part 3: Bulk Current Injection (BCI) Method

Part 4: Direct RF Power Injection Method



Conducted Methods

Part 5: Workbench Faraday Cage Method

IC-Level Test

These IEC stds are limited to 1 GHz. The demand for extended frequency range validity has motivated ongoing research **on more accurate tests**.

ISO 11452-4 (Part 4): Bulk Current Injection (BCI) Method

This std is limited to 400MHz.

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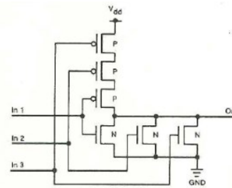
Existing Techniques to Protect Against (TID) Radiation

- *Use of guardbands: slow down clock frenquency, put extra timing margins*

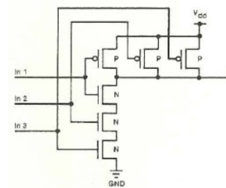
- *Prefer use of modern technologies (insead of old, mature ones): scaling down is always a good option since nanotechnologies (typically under 65nm) are strongly TID-tolerant*

- *Use of TID-tolerant std cells library (build-up pMOS devices much larger than nMOS devices, replace NOR gates by Nand ones, etc ....)*

CMOS circuit schematic:
(a) NOR gate; (b) NAND gate:



(a)



(b)

NAND gate has shown in Co^{60} tests to retain a higher degree of its original noise margins with radiation and is thus the preferred logic gate for hardened IC designs.

If NOR gates must be used in circuits designed for space, the # of inputs (i.e., the fan-in) should be minimized.

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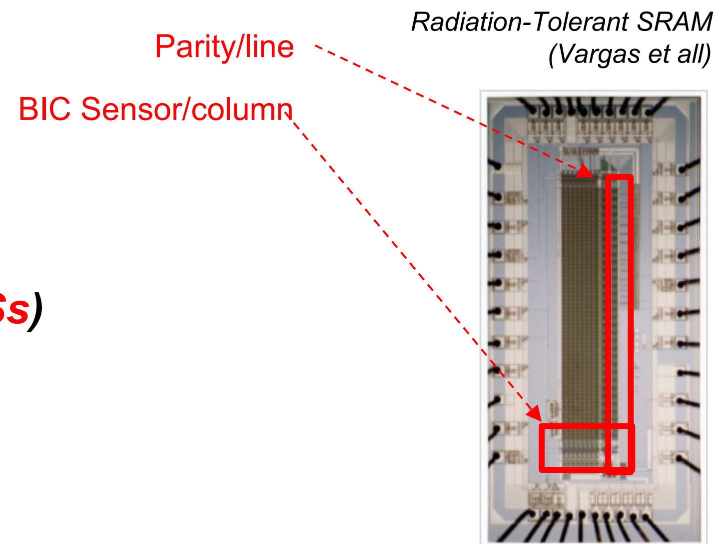
Existing Techniques to Protect Against (SEU) Radiation

- *Use of HW, SW, Time & Information (EDAC) Redundancy such as TMR, Functional Units Duplication with Comparator, Interleaving, etc ...*

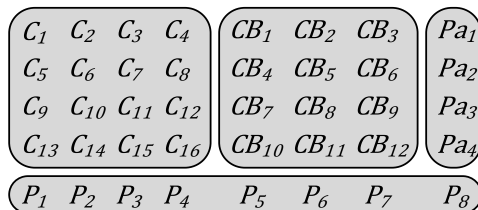
- *Use of Build-In Current Sensors (BICSs)*



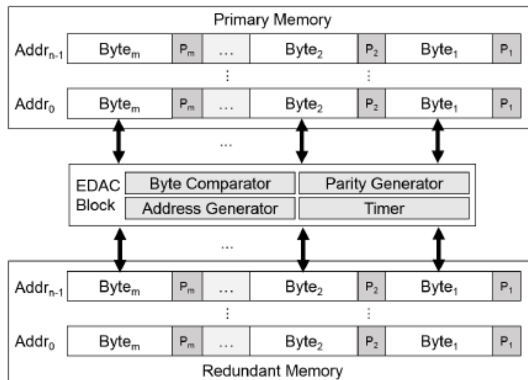
vargas@computer.org

Existing Techniques to Protect Against (SEU) Radiation

- *EDAC in Memory Array:* ***Parity,*** **Hamming Extended, Checksum, CRC, Reed-Muller, Matrix, CLC, ...**



Codified CLC word model

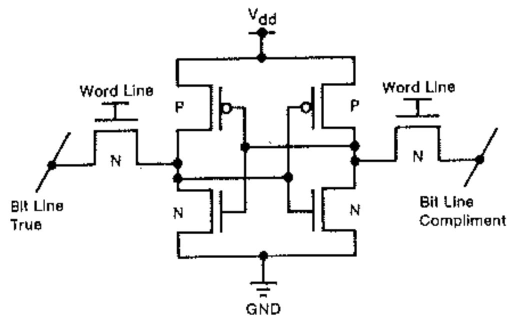


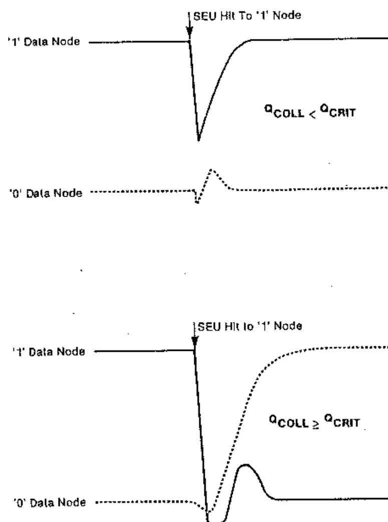
Parity-per-Byte and Duplication (PBD) Approach

Existing Techniques to Protect Against (SEU) Radiation

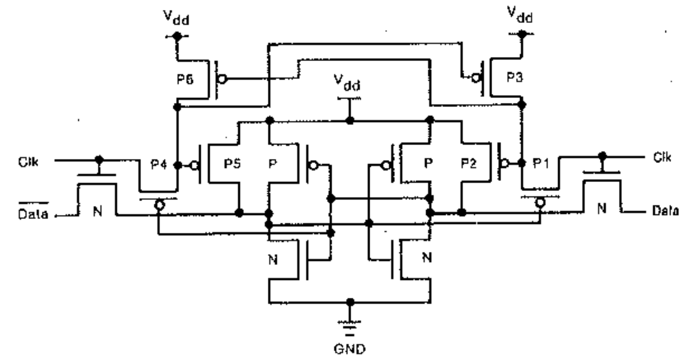
- Use of **SEU-tolerant std cells library**: design rad-hard SRAM cells

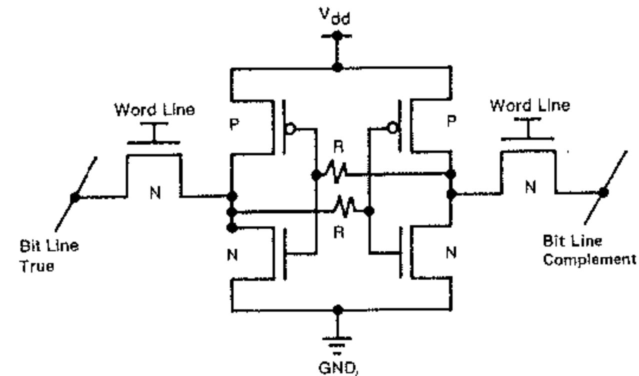
Classic CMOS SRAM cell schematic and the critical charge (Q_{crit}):





Design-hardened CMOS SRAM cell schematics:

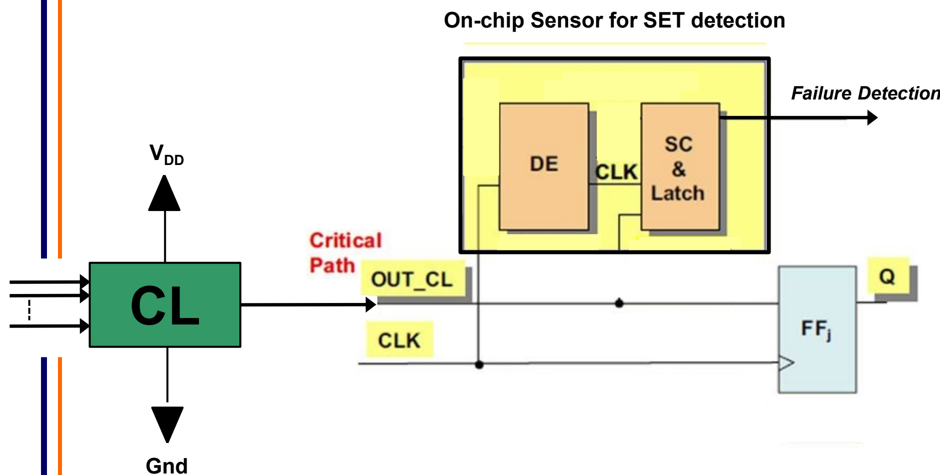




Existing Techniques to Protect Against (SET) Radiation (also valid for EMI, TID, Aging)

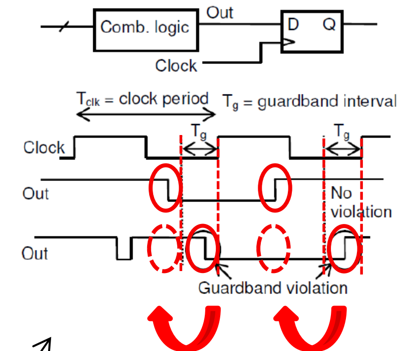
- Use of on-chip sensors at the output of critical paths to detect the occurrence of single-event transients (i.e., an unwanted glitch captured by a FF at the path output.

This approach is quite similar to the addition of on-chip aging sensors to predict circuit aging and then, recovery before failure occurrence.



Correct operation

Correct operation but not reliable



Sensor detects *guardband* violation during circuit operation.

According to the degree of perturbation detected by the sensor, it increases the **V_{DD} source**.

Can be implemented in FPGA or custon IC.

Process repeated till the end of the circuit lifetime.

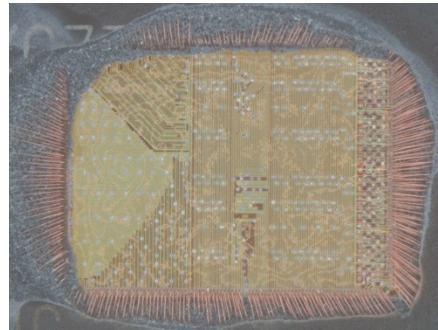
SiSC PUCRS

Existing Techniques to Protect Against (SET) Radiation (also valid for EMI, TID, Aging)

Developed Technique:

"Detection of aging in a Combinational Circuit by Slack Measurement in FPGA"

Poof of Concept on a Xilinx Zynq z7000
(Part N. XC7Z010-1CLG400C)



Existing Techniques to Protect Against (SET) Radiation (also valid for EMI, TID, Aging)

Detection of aging in a Combinational Circuit by Slack Measurement in FPGA
(proof of concept)

Circuit Aging Detection Based on Time Slack Measurement: a concept validation in FPGA

Jardel Silveira, Jarbas Silveira, Caio Amaral, Fabian Vargas

Federal University of Ceara
Pontifical Catholic University of Rio Grande do Sul

Existing Techniques to Protect Against EMI…

Increasing immunity to power supply fluctuations:

- On-chip decoupling “*power supply / core*” (near I/O ports):

(a) minimize transient currents and voltage swings (mainly on substrate, reducing Gnd bounce) and

(b) prevent external noise from entering power pins

Existing Techniques to Protect Against EMI…

Increasing immunity to power supply fluctuations:

- Perform a dedicated power distribution design by means of multiple paths to drive large amounts of current induced by fast logic switching activity ⇒ minimizes V_{DD}/Gnd bounce

- Design circuits to work within low operating frequency rates: use of guardbands to increase noise margins

- Design of asynchronous logic by migrating existing clocked architectures or designing new ones ⇒ intrinsically delay-insensitive

DLX Processor (ASPIDA Project - Asynchronous Open-Source Ip of the Dlx Architecture)
(http://www.ics.forth.gr/carv/async/demo/)

Asynchronous Circuits and Systems Group of Institute of Computer Science – FORTH, University of Crete, and Microelectronics Group of Politecnico di Torino

SiSC PUCRS

1. Understanding the effects of ionizing radiation (TID, SEU, SEE) & non-ionizing radiation (EMI) on embedded electronics

2. Mitigation techniques

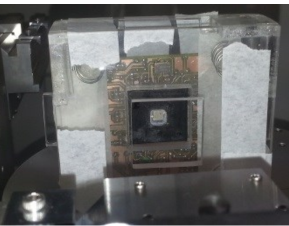
3. Combined test planning

4. Configurable platform and lab requirements for combined test

5. Experiments combining TID + SEU + EMI tests on FPGAs

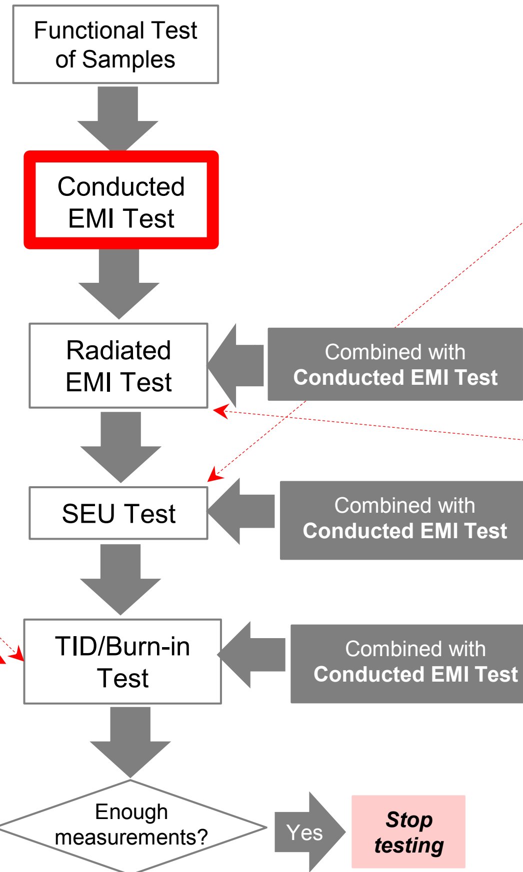
Combined Test Planning Methodology

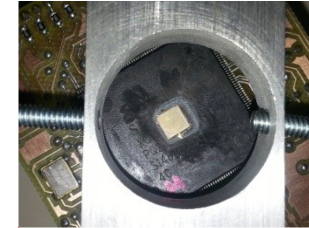
Combined tests: *EMI + Radiation*



X-Ray

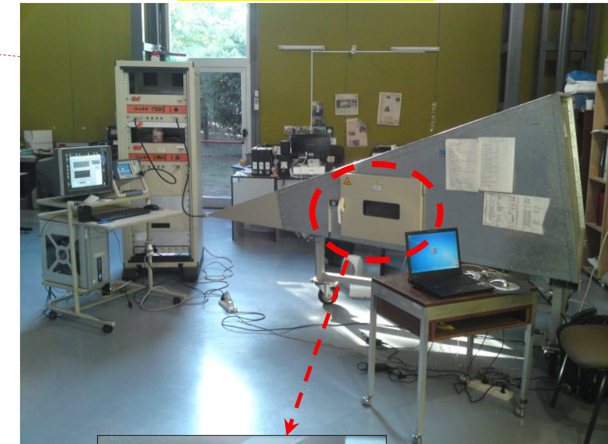
Co^{60} (Gamma Cell)





SEU

Radiated EMI Test (G-TEM Cell Test Method)



1. Understanding the effects of ionizing radiation (TID, SEU, SEE) & non-ionizing radiation (EMI) on embedded electronics

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Goal

In this context…

We have been developing a **configurable platform suitable for combined tests of EMI, radiation and aging measurements** of prototype embedded systems

☞ The platform can be used to perform measurements on ICs and embedded systems having in mind EMI and radiation international stds:

- IEC 62.132-2 (for radiated EMI noise)
- IEC 61.0004-17 and IEC 61.0004-29 (for conducted EMI noise)

and

- TID: 1019.4 & 1032.1 methods for (TID & SEU Test Procedures of MIL-STD-883H)

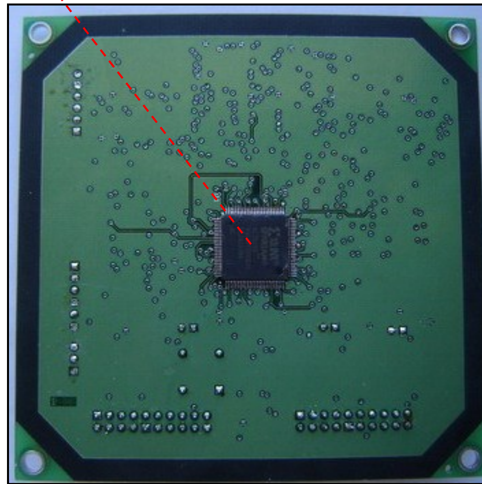
SiSC PUCRS

Platform (HW parts)

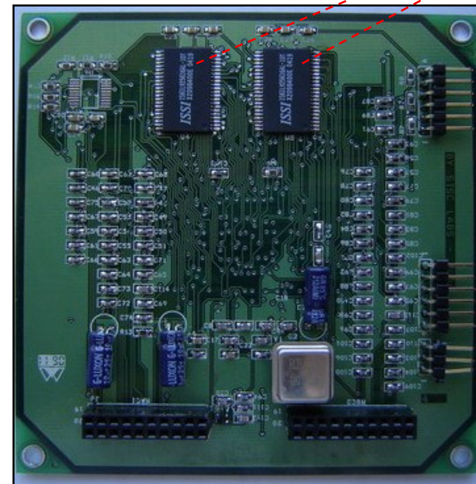
FPGA (System-on-Chip)

16MB SRAM (RTOS
+
user application)

System under Test



Top view



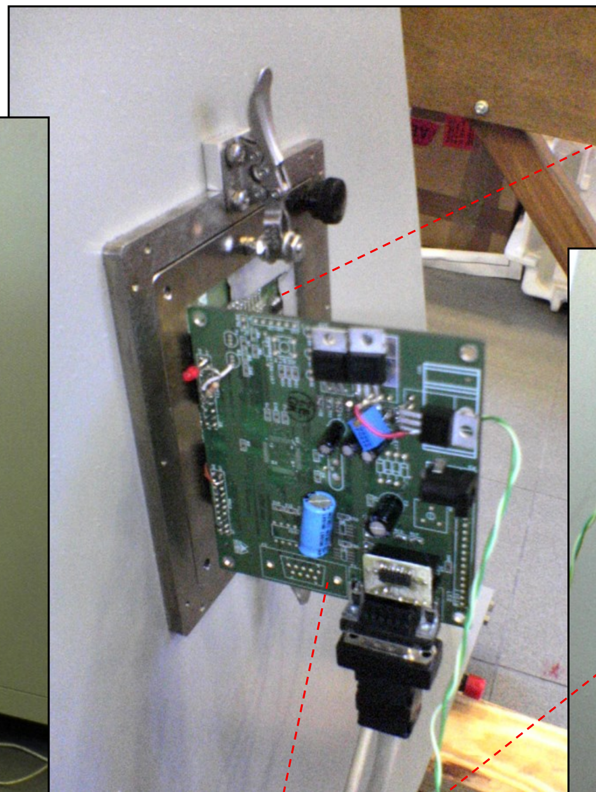
Bottom view

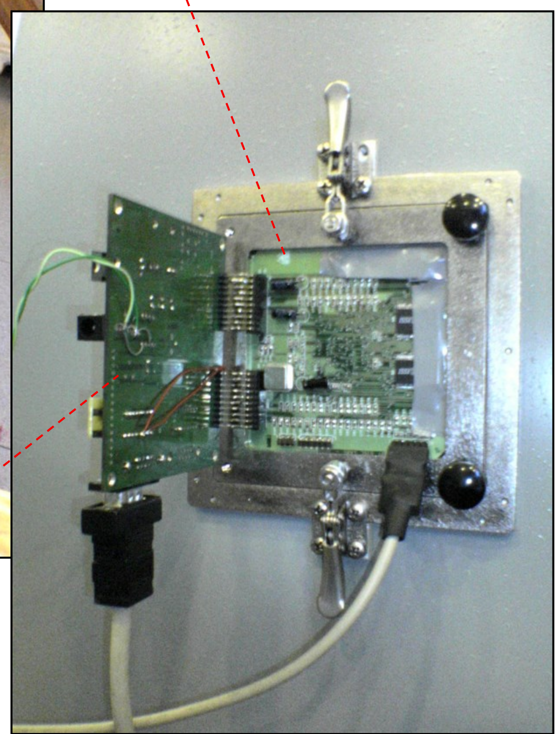
IEC 62.132-2 std compliant board.

Four-layers: Gnd (top) - signal - signal - Vdd (botton).

1st

Platform (HW parts)



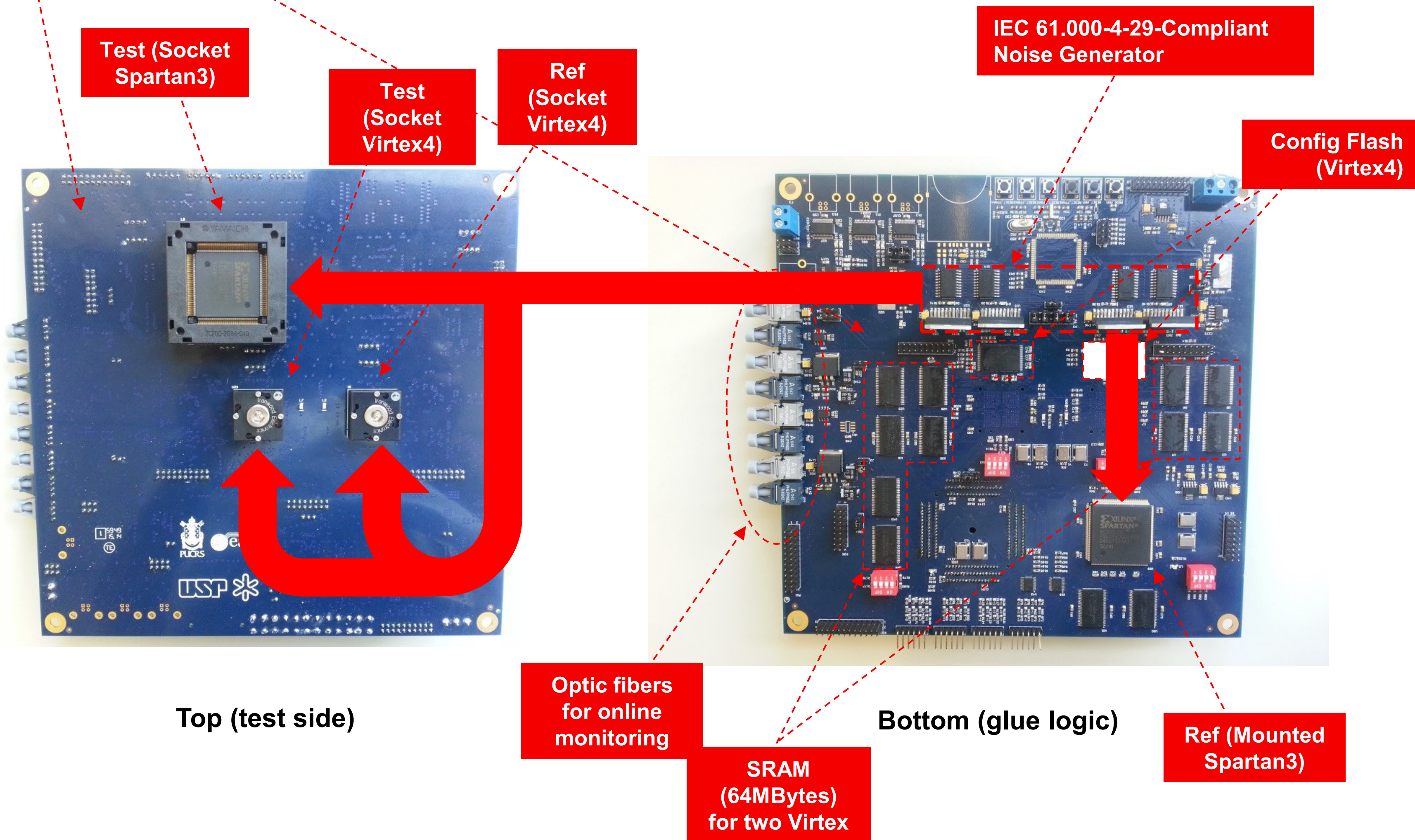


System under Test

Interface Board

TEM Cell

Platform (HW parts)



12-layer Motherboard for Combined EMI x Radiation tests

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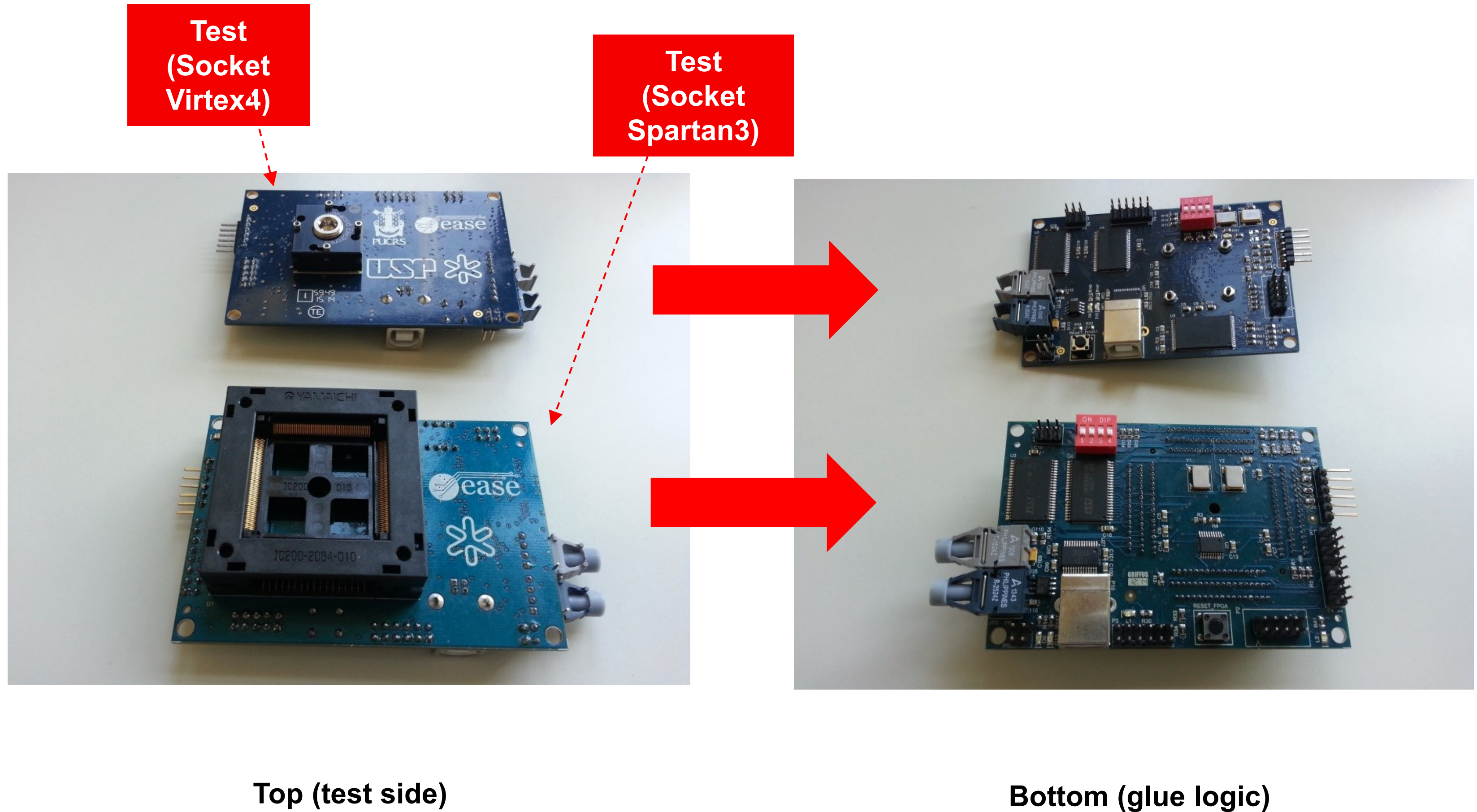
Platform (HW parts)



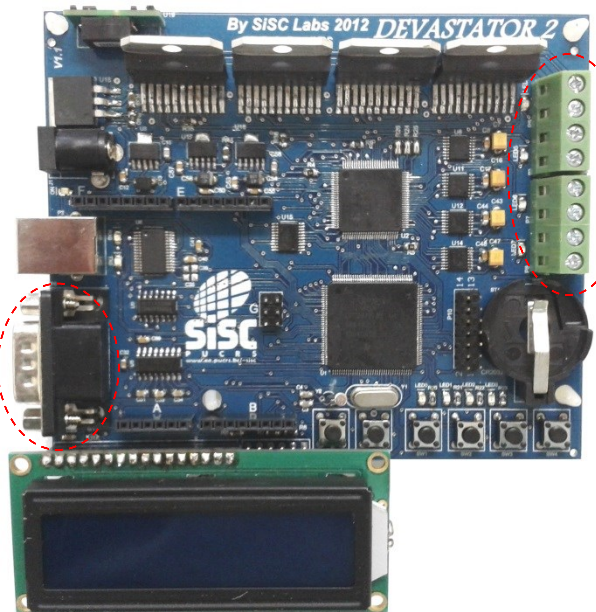
Top (test side)

Bottom (glue logic)

6-layer Daughterboards for Combined EMI x Radiation tests

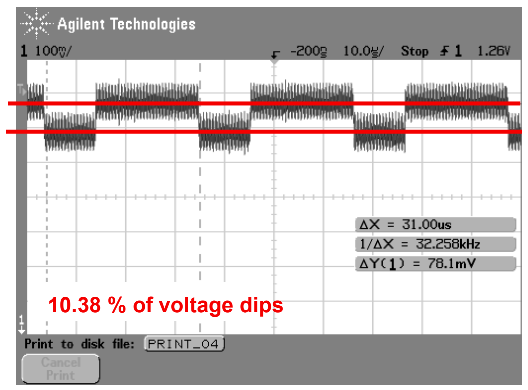
Platform (HW parts)

IEC 61.000-4-17 and -29 Compliant External EMI Noise Injector



Power-Supply to the CUT

Configurable from PC (Serial port)



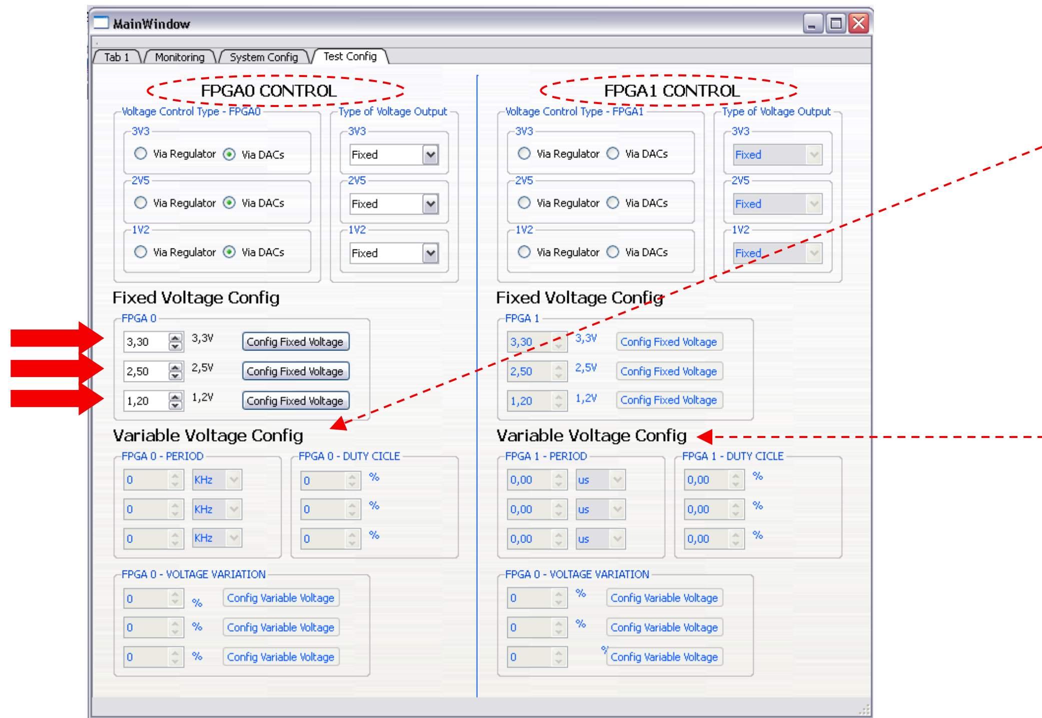
1.2 volts

1.07 volts

10.38 % of voltage dips

Conducted noise injected in the CUT

Platform (SW parts)



Test Type	Level	Percentage of the nominal DC voltage
Ripple	1	2
	2	5
	3	10
	4	15
	X	X

Test Type	Test Level (%)	Duration (s)
Voltage Dips	40, 70 or X	0.01
		0.03
		0.1
		0.3
		1
		X

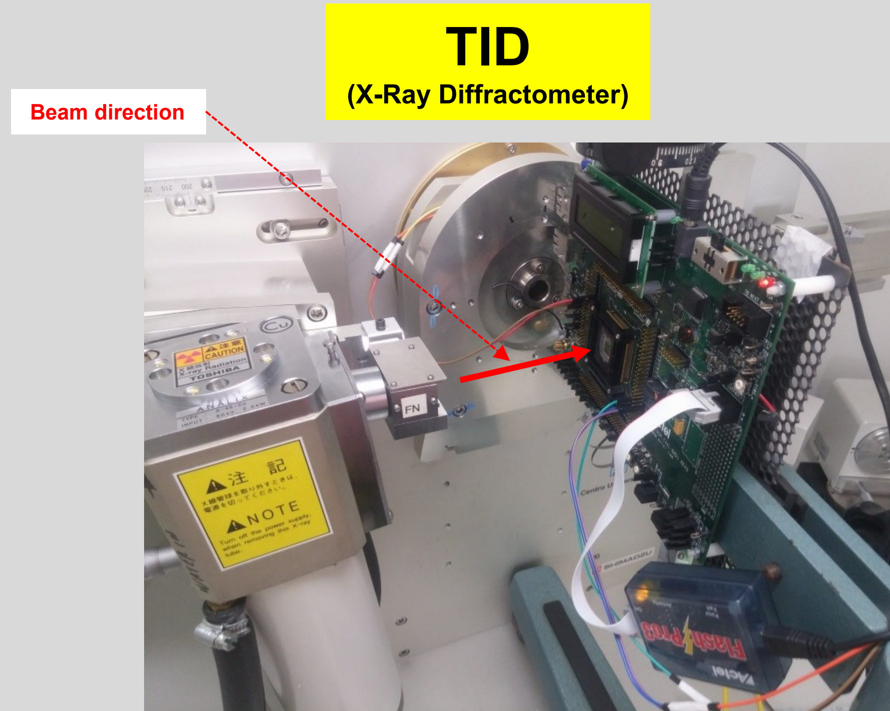
Programming interface of the platform:
Screenshot of the configuration environment to perform tests according to the IEC stds 61.000-4-17 and 61.000-4-29

Laboratory Setup

Microsemi ProAsic3E1500

Goal:

SEU sensitivity w.r.t. V_{DD} Disruption and TID



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Combined Tests:

Conducted EMI with TID

Experiment (1)

IP Core: RTOS-Guardian (RTOS-G), a watchdog to monitor RTOS activity in embedded systems

☞ **the RTOS-G targets faults that ESCAPE detection by the native structures present in the RTOS kernel.**

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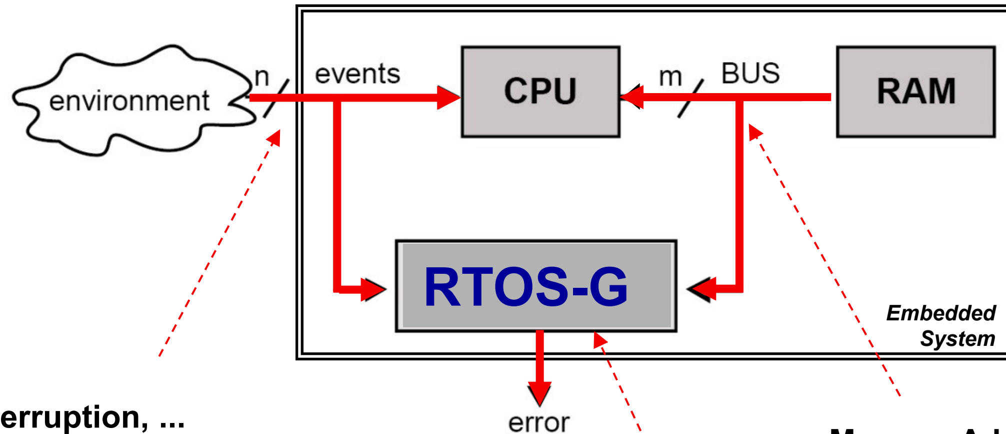
Experiment (1)



Events: Tick, interruption, ...

(Reference for

Task Context Switching)

Memory Addresses accessed by the processor.

RTOS-G identifies the current task under execution by correlating addresses flowing through the bus with the information stored in an Address Table generated during the compilation process.

Block diagram of the target embedded system

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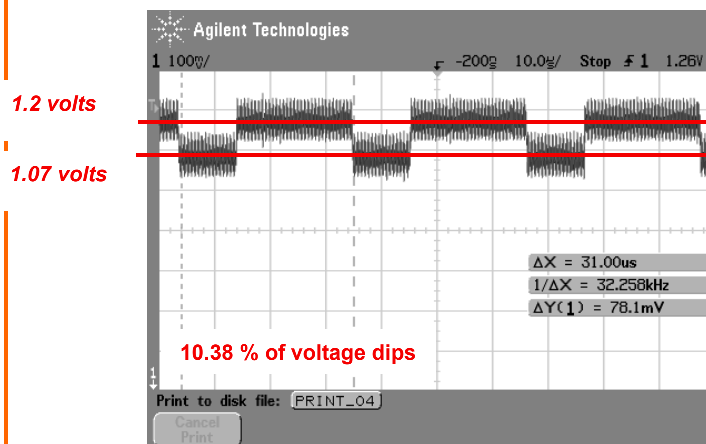
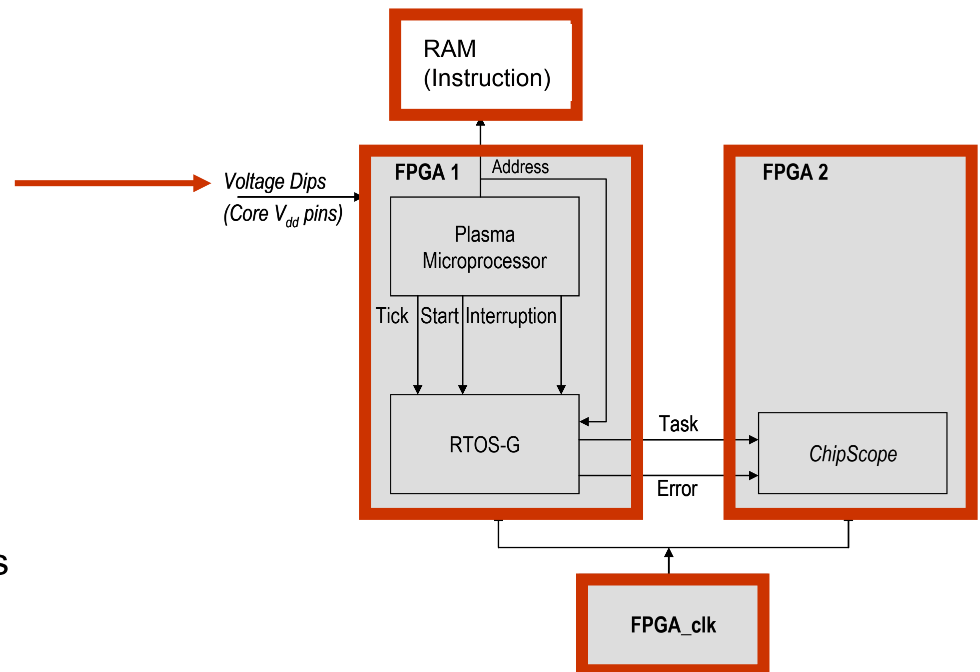
Experiment (1)

Fault injection campaign: ***generated according to the IEC 61.000-4-29 Int. Std. for conducted EMI on the DC input power port of (fresh) FPGA 1***

Voltage dips were randomly injected at the **FPGA 1 V_{dd} input pins** at a frequency of **25.68 kHz** and consisted of dips of about **10.83% of the nominal V_{dd}**.



Injected noise at the FPGA power bus (conducted EMI)



Fault injection environment

Experiment (1)

Results for Fault Detection

As long as more complex services of the kernel are used, the higher is the RTOS error detection.

*The native fault detection mechanism (**assert() function**) is called by the kernel every time RTOS runs its services (message queues, semaphores).*

Benchmark	RTOS Kernel [%]	RTOS-G [%]
BM1	2.40	99.90
BM2	25.90	100.00
BM3	45.80	100.00
Average	***24.70***	***99.97***

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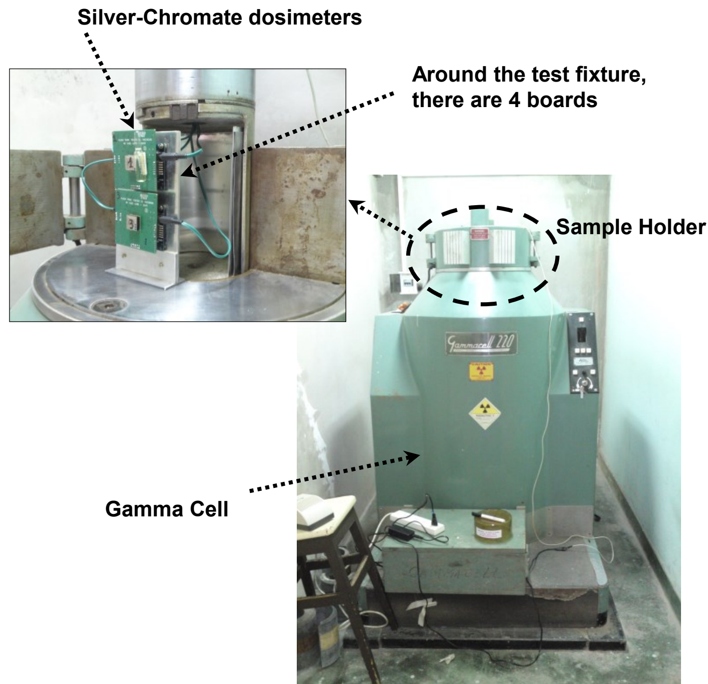
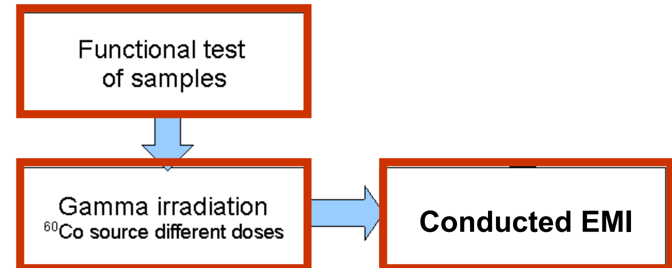
Experiment (1)

Fault injection campaign: *TID irradiation of FPGA1 in a Gamma Cell with Co^{60}*





Experiment	FPGA0 (krads)	FPGA1 (krads)	FPGA2 (krads)	FPGA3 (krads)	FPGA4 (krads)
1st experiment	0	5.6	51.9	111.0	216.0
2nd experiment	0	217.6	263.9	323.0	---

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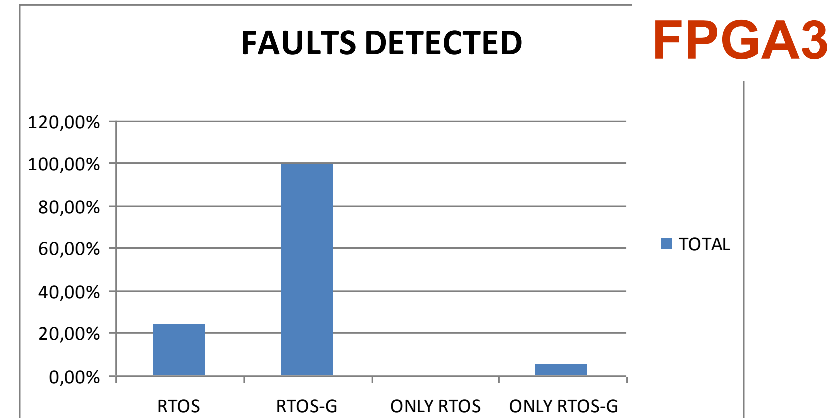
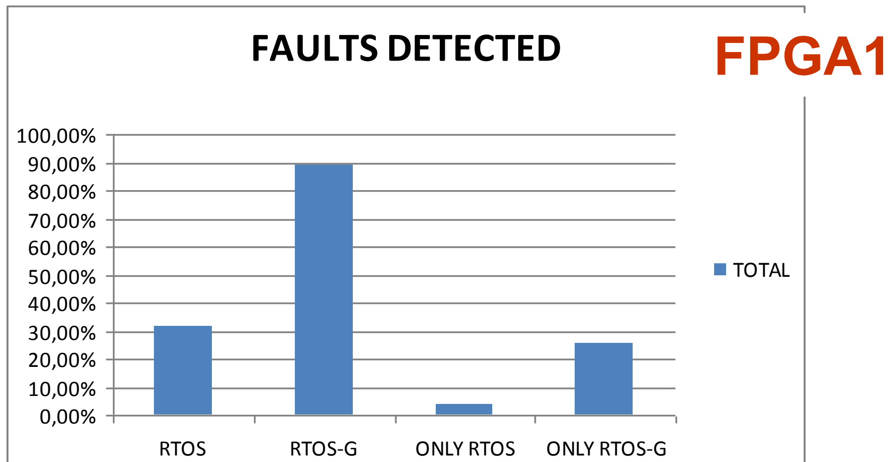
Experiment (1)



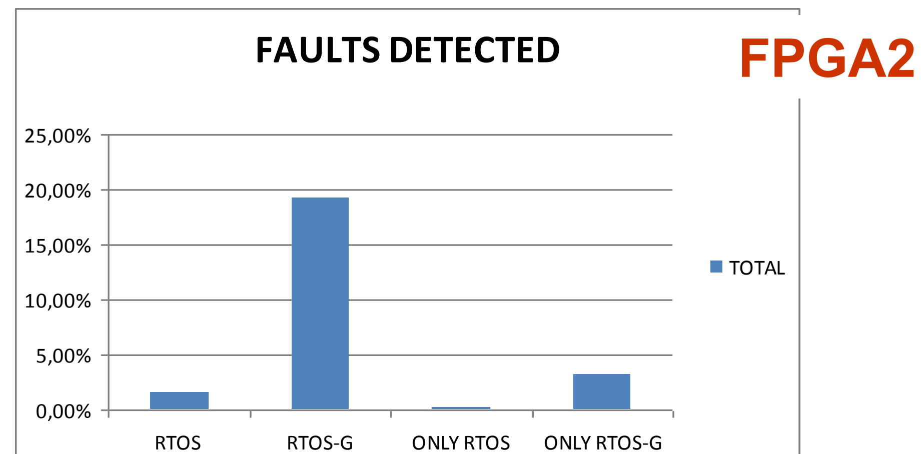
FPGA3



FPGA1

RTOS-G: 68,67%

RTOS: 18,00%



FPGA2

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Combined Tests:
Radiated EMI with TID

Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity

1st Part*: **4 fresh FPGAs Virtex4** (XC4VFX12-10SF363) were characterized to radiated EM Immunity.

* *based on **IEC 61.132-2 Std** (TEM Cell Method).*

Test method conditions:
- EM field range: from 10 to 120 v/m (volts/meter);
- Radiated signal frequency range: [150kHz - 1GHz];
- Signal modulation: AM Carrier 80% modulation at 1kHz, Horizontal Polarization.

2nd Part**: aging by TID exposition:

- *Fab.* ***Lot 1****:* 2 FPGAs received a total dose of **160 krads**
- *Fab.* ***Lot 2****:* 2 FPGAs received a total dose of **336 krads**

** *based to **MIL-883H Std** (1019.8 Method for TID radiation testing), room temperature, dose rate: 155.5 rads/s.*

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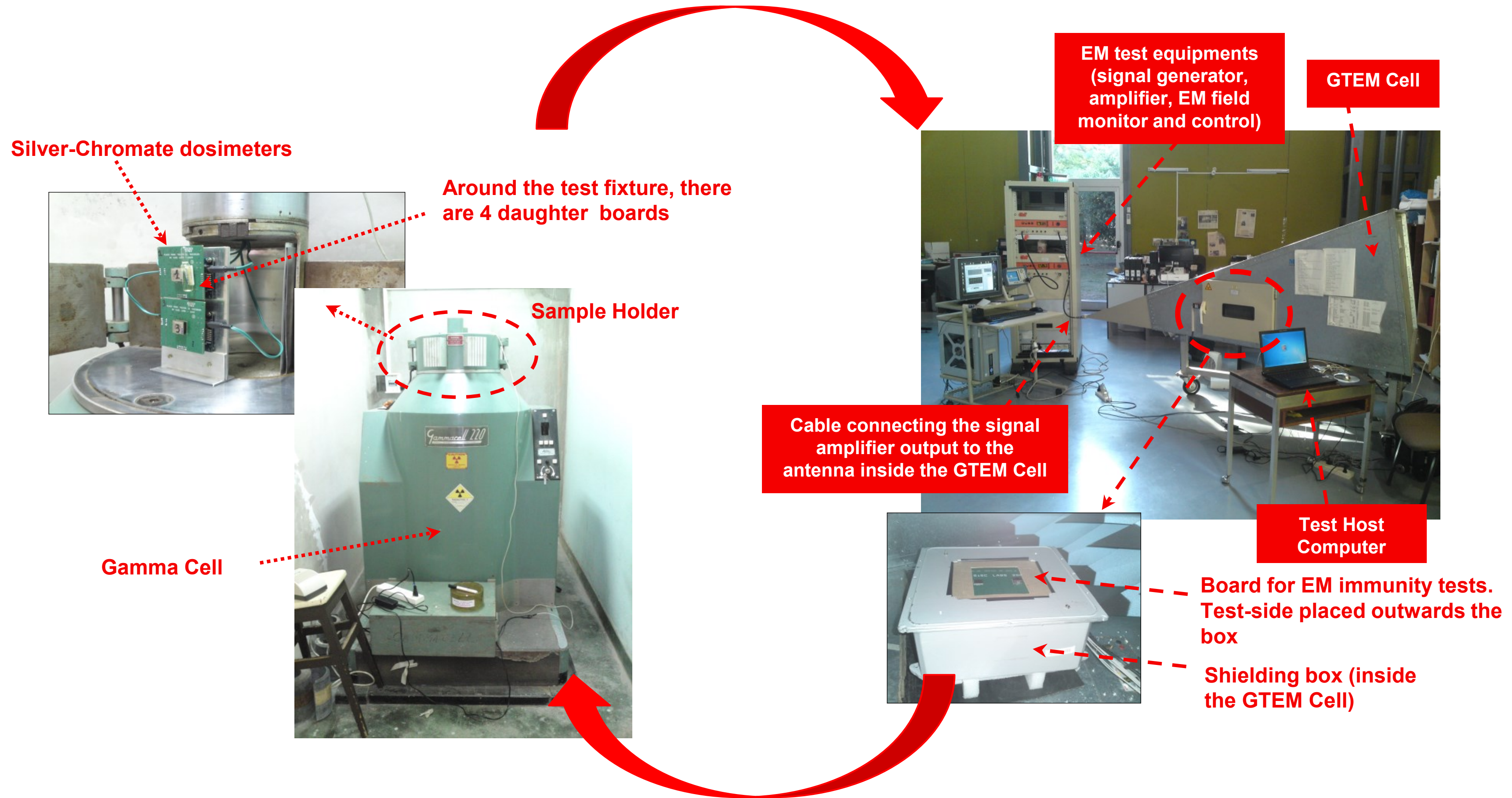
Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity



Radiation source used for gamma radiations.

Environment for radiated EM immunity measurements.

Test Environment

SISC PUCRS

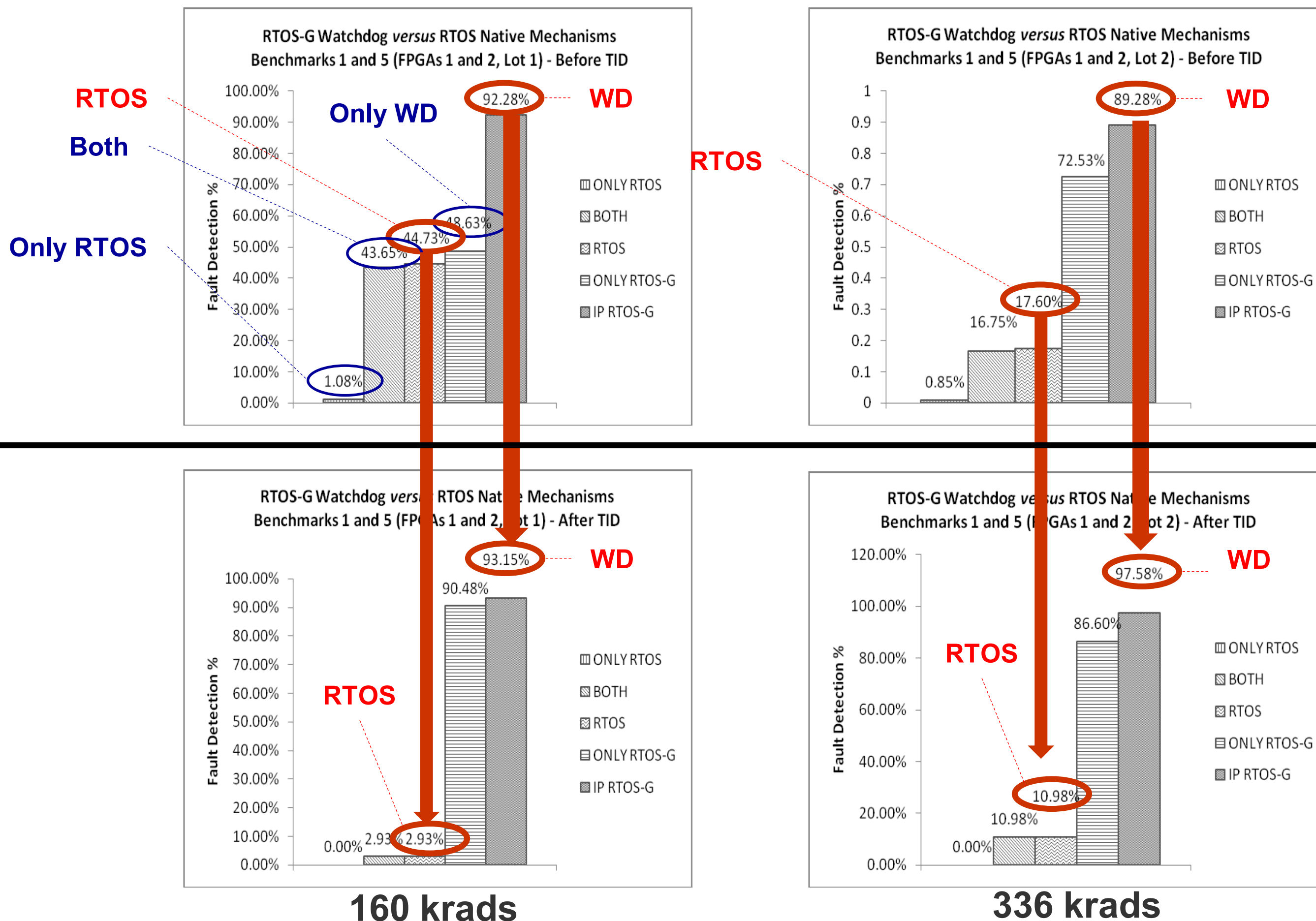
Experiment (2)

Combined tests:

TID (Co^{60}) and Radiated-EM Immunity

irradiated EMI, before TID

irradiated EMI, after TID



Comparison between the fault detection capability of the WD against the RTOS native fault detection mechanisms for fresh and aged FPGAs operating in an EMI-exposed environment

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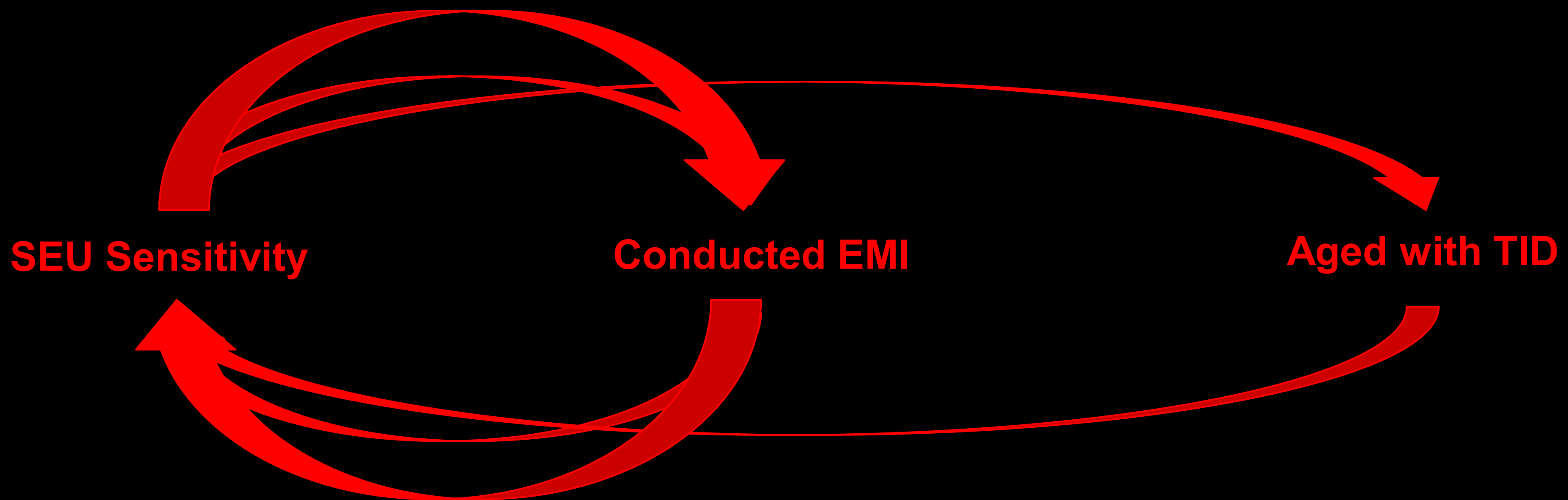
Combined Tests:

Conducted EMI with TID and SEU



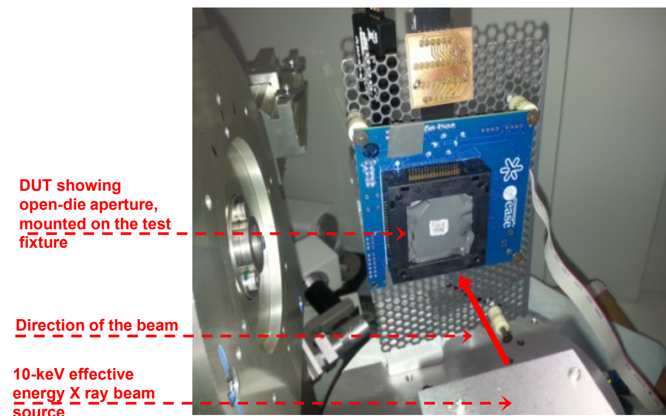
Experiment (3)

Goal:

SEU sensitivity as a function of V_{DD} Disruption and TID

TID

(X-Ray Diffractometer)

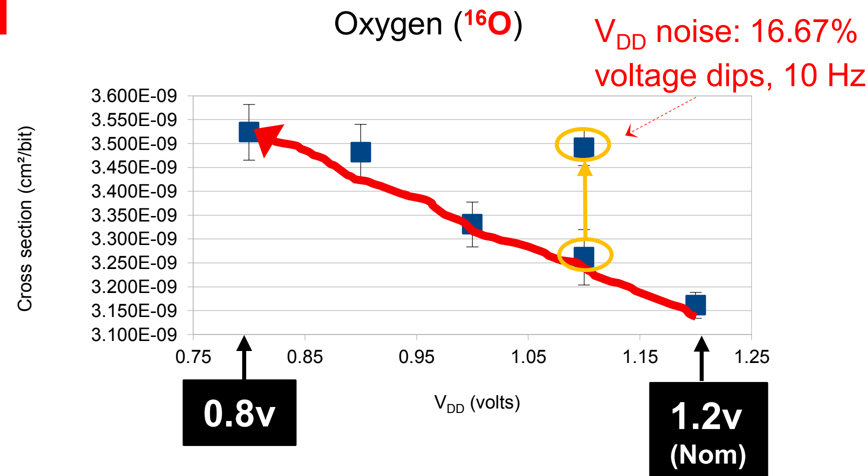


Experiment (3)

(Configuration Bitstream) SEU sensitivity as function of Noise on Power Supply (V_{DD})
(Fresh FPGA)

SEU sensitivity (σ): +10% w.r.t. nominal V_{DD}

SEU sensitivity (σ): +11% w.r.t. nominal V_{DD}



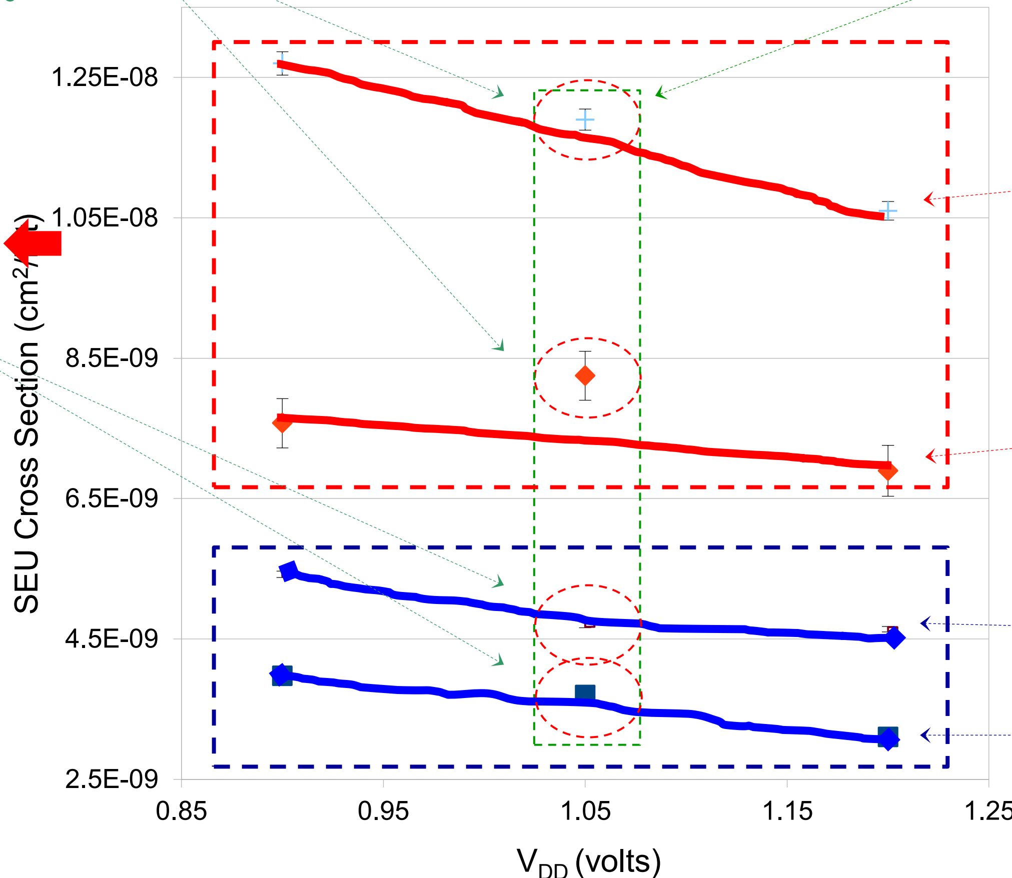
Experiment (3)

(BRAM vs. Config) SEU sensitivity
as function of Noise on Power Supply (V_{DD} Core) and TID

SEU sensitivity degradation w.r.t. the nominal V_{DD}: 16%

SEU sensitivity degradation w.r.t. the nominal V_{DD}: 10.4%

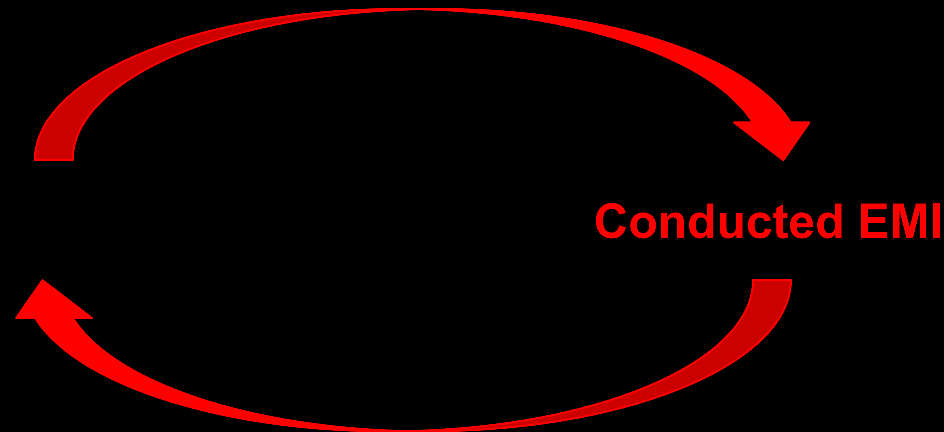
BRAM ~ x4.3 more sensitive to SEU than Config mainly due to the imprint effect



PS: TID deposited with all BRAM cells storing "0s" (the hard pattern)

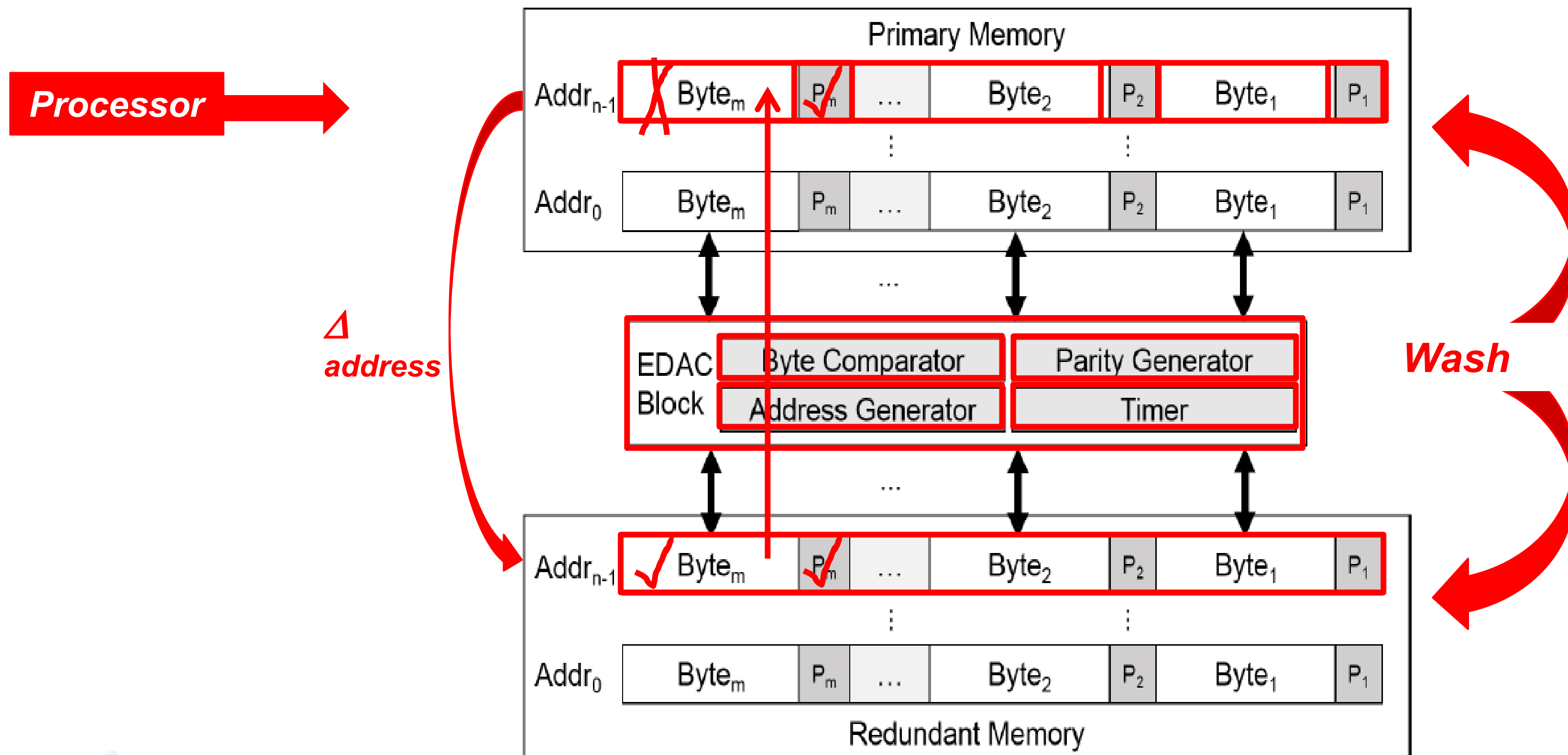
Combined Tests:

Conducted EMI with SEU



Experiment (4)

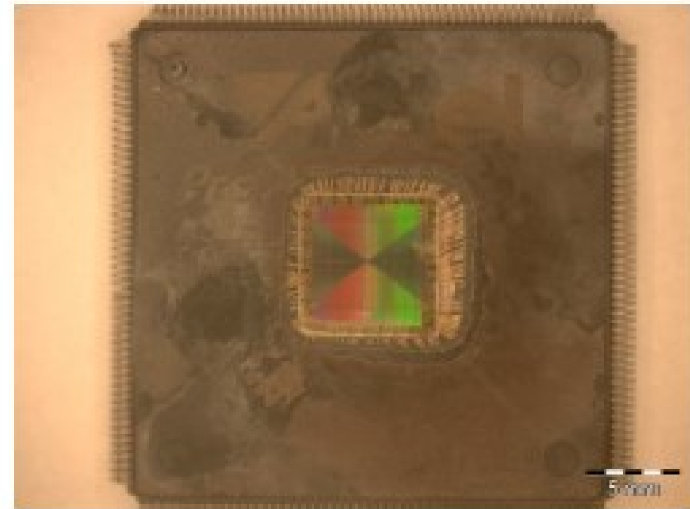
Parity per Byte & Duplication (PBD) EDAC Technique



General block diagram of the proposed EDAC approach.

Experiment (4)

(a)



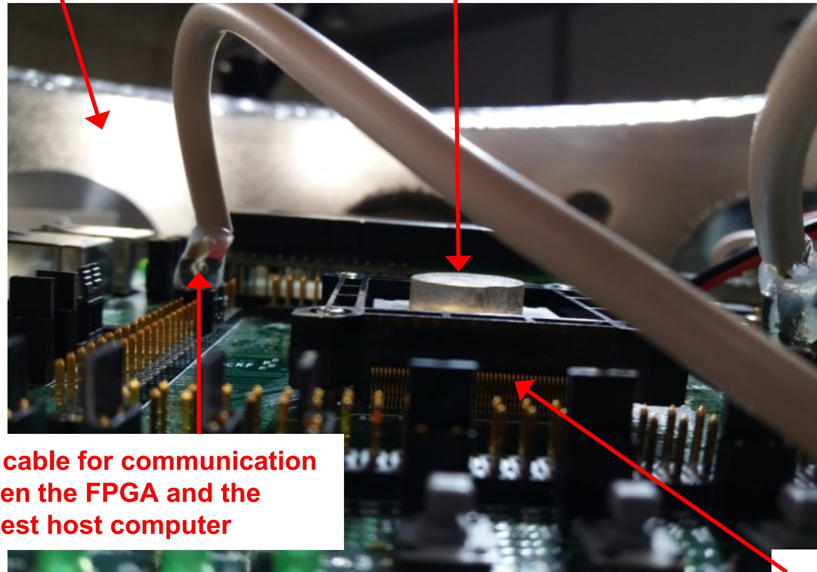
(b)

Microsemi ProAsic3E A3PE1500 FPGA:
(a) Packaged device;
(b) Unpacked, ready for radiation (SEU and TID) tests.

(commonly used for automotive and aerospace apps)

Experiment (4)

SEU Test:



Test setup for the ^{241}Am source

ProASIC3E FPGA exposed to 5.4 MeV alpha particles emitted by a ^{241}Am source

Alpha-particle flux:.
Appr. 1,300 part/cm^2.s
(13.7 particles/second /millisteradian)

Experiment (4)

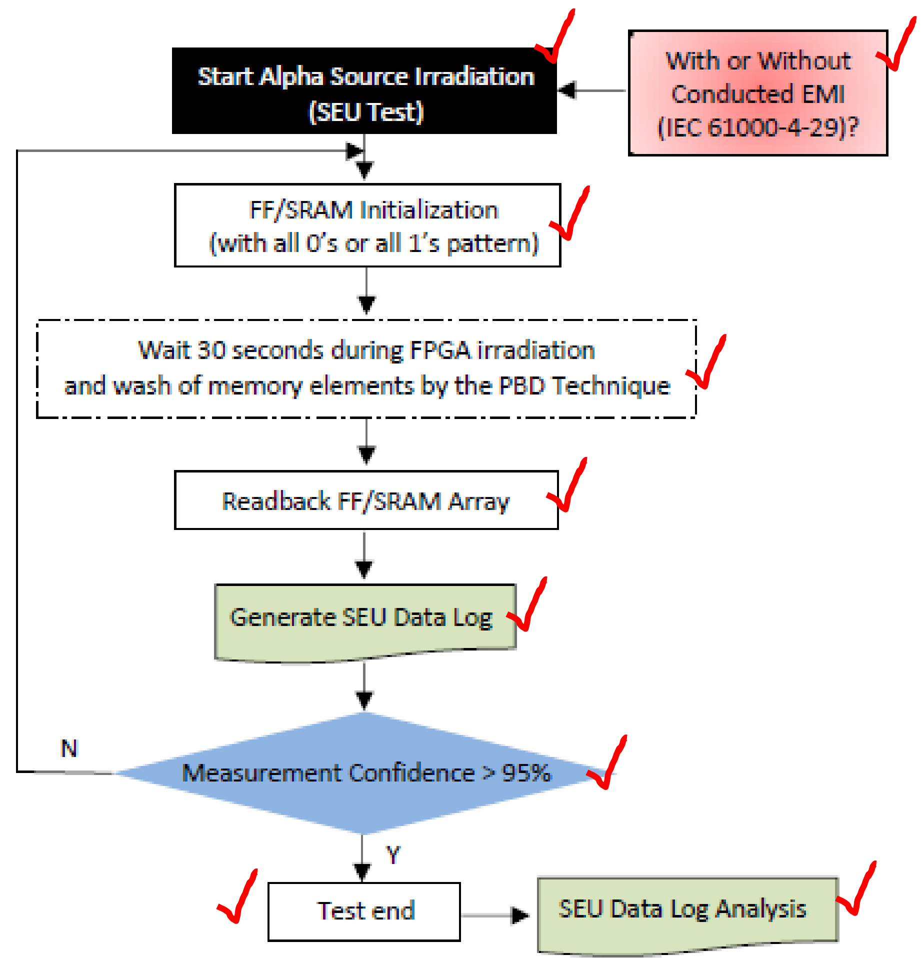
Combined Test for SEU/Conducted EMI

PROASIC3E OCCUPIED RESOURCES

FPGA Hardware Summary	Core Logic (VersaTiles)	FFs	SRAM Cells
Used hardware configuration	37,903	18,432	276,480
Max. hardware available	38,400	38,400	276,480

100%

48%



Test Flow

Experiment (4)

EMI Test:

Fault injection campaigns were generated according to the IEC 61000-4-29 Std

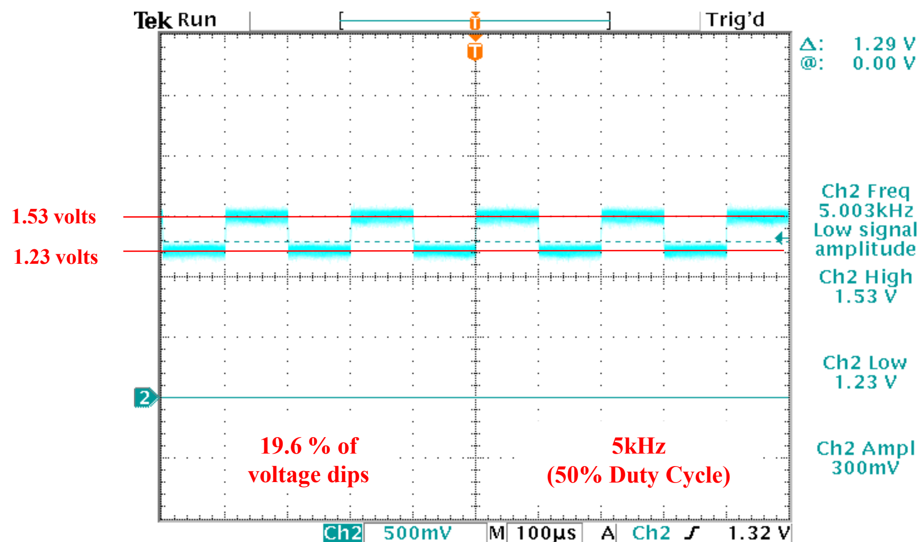


Fig. 6. Noise injected on FPGA V_{DD} pins.

Voltage dips applied to the FPGA core V_{DD} pins (Nominal core V_{DD}: 1.5 volts)

IC peripheries remained fixed at their nominal voltage levels (3.3, 2.5 and 1.8 volts)

Experiment (4)

Obtained Results

TABLE II.
CAPABILITY OF THE PBD TECHNIQUE TO MITIGATE SOFT ERRORS INDUCED BY ALPHA PARTICLES, WITH AND WITHOUT CONDUCTED EMI NOISE ON THE CORE INPUT POWER PORT OF THE FPGA.
RESULTS FOR THE SRAM ARRAY.

PBD TECHNIQUE EFFECTIVENESS TO ALPHA PARTICLES, WITH AND WITHOUT CONDUCTED EMI NOISE ON INPUT POWER PORT			
Average number of...	Without Noise	With Noise	Soft Error Increase*
observed bit-flips	395.00	1,049.00	2.7
bit-flips per memory bits	0.0027	0.0071	2.6
bit-flips per second	0.4760	1.0708	2.3
bit-flips per memory bits per second	0.0028	0.0073	2.6
addresses corrected**	393.33	1,044.37	2.7
addresses not corrected	0.17	0.63	3.7
masked addresses***	0	0	0
EDAC Effectiveness (%)	99.96	99.94	

*"Soft Error Increase" rate computed as: With Noise/Without Noise.
**the number of addresses corrected is smaller than the number of observed bit-flips because there was at least one address with more than one bit flip.
***masked addresses are addresses not detected and not corrected, thus escaping detection by the proposed technique.

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Experiment (4)

Obtained Results

Compared to only ionizing radiation, when the IC was additionally exposed to conducted EMI,
FF & SRAM arrays became
~ 2.7 times more sensitive to soft errors

Experiment (4)

We can compute the required Δt (wash time interval) for a given expected mean-time before failure (MTBF):

MTBF: in order to calculate a conservative MTBF we assume the system lifetime should be 10 times greater than the lifetime desired for the target system.

*If a system lifetime of 15 years is desired, then a reasonable MTBF of 150 years (**5.475×10^4 days**) is assumed.*

*Assume also that the FF and SRAM arrays store a relative sensitive data for which we could not accept more than **5 errors** over the whole mission time.*

*Therefore, the target **MTBF = 10,950 days** ($5.475 \times 10^4/5$)*

Since MTTF = $1/\lambda$: the Failure Rate λ **= 9.13×10^{-5} errors/bit-day**

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Experiment (4)

FPGA Parameters:

a) Word size: 16 bits (+ 2 parity bits) = 18 bits

b) SRAM capacity: 276,480 cells/18bits = 15,360 18-bit words

c) FF capacity: 38,400 FF/18bits = 2,133 18-bit words

Wash interval Δt = ? *(to be computed …)*

Experiment (4)

And the reliability model is defined as follows ...

Now, assume that the probability of an upset in a single bit, after time Δt, can be obtained by using the following relation:

$$P_{1,1} = 1 - e^{-\lambda \Delta t} \qquad \text{(I)}$$

(where $e^{-\lambda \Delta t}$ is the survival probability in $\lambda \Delta t$ days for a single bit)

Assuming that the probability $P_{1,1}$ is the same for each bit, and the occurrence of an error in a bit is independent of the occurrence of errors in any of the other bits, the probability of r errors in n bits is given by the binomial distribution:

$$P_{r,n} = C_{n,r}.P_{1,1}^{r}.(1 - P_{1,1})^{n-r} \qquad \text{(II)}$$

(where $C_{n,r}$ denotes the number of combinations of r errors in n bits)

Initially, the code word is error free. After time Δt, the probability that the code word is correct is:

$$R_1(\Delta t) = 1 - P_{r,n} \qquad r = d + 1 \qquad \text{(III)}$$

(where d is the number of errors which can always be detected)

After N intervals of Δt, the probability that the code word is correct is:

$$R_1(N\Delta t) = [1 - P_{r,n}]^{N} \qquad \text{(IV)}$$

Assuming independence of the code words, the reliability of a system of W code words after time $N\Delta t$ is:

$$R_w(N\Delta t) = [1 - P_{r,n}]^{NW} \qquad \text{(V)}$$

The expected life of the system, which is referred to as mean time before failure (MTBF), is defined by the equation:

$$MTBF = \int_0^\infty R_w dt \quad \text{(where } R_w \text{ is the reliability of the system)} \qquad \text{(VI)}$$

Noting that $N = t/\Delta t$, then:

$$R_w(N\Delta t) = \{[1 - P_{r,n}]^{W/\Delta t}\}^{t} \qquad \text{(VII)}$$

which when substituted into (VI), yields the solution:

$$MTBF = \frac{-\Delta t}{W.\ln[1 - P_{r,n}]} \qquad \text{(VIII)}$$

work in progress

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Thank you for your attention …